MIL/COTS DIGEST

The Defense Electronic Product Source

Fall 2010

In This Issue

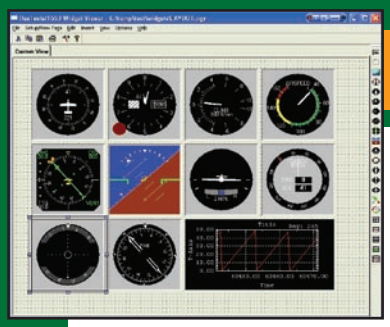
VME's VPX progeny will dominate in 2011

In the past 12 months, the high end of the VME ecosystem has gone from the latest FPGA-based PMC/XMC mezzanines on conduction-cooled 6U VME boards to deployed 10 GbE 3U VPX and OpenVPX switches. In October 2009, the OpenVPX Working Group handed its collaborative work over to VITA, giving rise to the official VITA 65 OpenVPX standard. Earlier this year, it was ratified by ANSI and is now an international standard. With so much accelerated effort by so many individuals and companies, as well as millions of dollars of engineering investment, the VME ecosystem now consists of countless VPX and OpenVPX boards, backplanes, and systems. Presented herein are 32 new VME, VXS, VPX, and OpenVPX products. Watch for VPX to dominate new products in 2011.

As always, PMC and XMC mezzanine modules provide additional capabilities onto baseboards. You'll find two PMC products and one XMC – the latter an interesting mix of A/D and D/A input/output ports. There are also many dedicated fabric "switch" cards (not counting fabric I/O already included on other boards). The most popular choices are Serial RapidIO and Fast Ethernet. You'll find two chassis – increasingly these are VPX chassis – along with two VPX development systems that include chassis. You'll also find several purpose-built systems and SBCs, including one from Mercury Computer Systems designed solely for ISR applications and one certifiable to DO-254.

And lastly, one of my favorites isn't a VME, VXS, or VPX product at all. It's a proprietary Atom-based Small Form Factor (SFF) module. I chose this one because VITA sees itself getting into the SFF business within the next 24 months with a completely new board size. I hope you enjoy these 32 selections.

Chris A. Ciufo, Editor
cciufo@opensystemsmedia.com

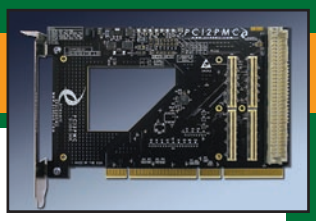


"Intuitive" GUI for 1553 data bus traffic

GE Intelligent Platforms' BusTools-1553 version 7 "Intuitive" GUI simulates, tests, and analyzes 1553 data bus traffic on CompactPCI, PCI, VME, VXI, PC/104, and PC/104-*Plus* form factors, among others. It hastens bus traffic analysis and monitoring and facilitates fast message modification and creation. It enables simultaneous multiple-bus control in addition to error detection/injection and speedy filtering for either recorded or live displayed data. The Dynamic Bus Monitor stop/start feature enables users to achieve efficient on-the-fly 1553 bus traffic routing. Additionally, a one-page bus list editor replaces the multi-page editor. Meanwhile, a Selective Data Watch feature lets readers choose different data words from any bus message to identify elusive system issues, thanks to integrated high/low limit checking, automatic limit event logging and corresponding snapshot feature, and DDE output.

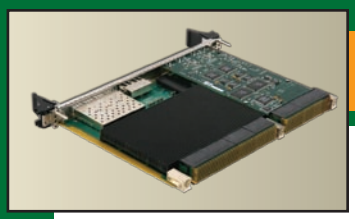
www.ge-ip.com **GE INTELLIGENT PLATFORMS**

PCI-to-PMC adapter



Dynamic Engineering's PCI2PMC PCI-to-PMC adapter enables PMC card installation into either a half-length or standard PCI slot at 6.600" per the PCI specification, meaning it's an adaptable half-length ware with universal voltage. The adapter provides a passive design and 33/66 MHz bus operation, along with 32-/64-bit data transfers. PCI2PMC supports 3.3 and 5 V PCI bus signaling, and +3.3, +5, +12, and -12 V can be supplied from the PCI backplane to the PMC with an optional jumper for PCI or a regulator at 3.3 V. Front- and rear-accessible connectors including a rear DIN64/SCSI connector are also proffered, and a cut-out design enables increased airflow. The adapter operates at -40 °C to + 85 °C and renders 4.6 million hours of MTBF. Additionally, an RoHS version is available.

www.dyneng.com **DYNAMIC ENGINEERING**



VPX Serial RapidIO Gen-2 switch

Curtiss-Wright Controls Embedded Computing's VPX6-6902 6U VPX Serial RapidIO Gen-2 Switch is a combined management, control, and data plane switch. Its 6U VPX/OpenVPX form factor supports star and dual-star topologies, and it is available with Serial RapidIO switch fabric alone or as combined Serial RapidIO and Ethernet switches in a single slot. It has 20/24x Serial RapidIO 4-lane (x4) ports to the VPX backplane + 4x ports to the front (AC only). Additionally, each Serial RapidIO port can operate at Gen-1 speeds of 1.25, 2.5, and 3.125 Gbaud or Gen-2 speeds of 5 and 6.25 Gbaud. Also proffered are 16x SERDES GbE and 2x 1000BASE-T to the back and 2x 10 GbE and 1x 1000BASE-T to the front. An onboard management processor for both Serial RapidIO and GbE fabrics is also provided.

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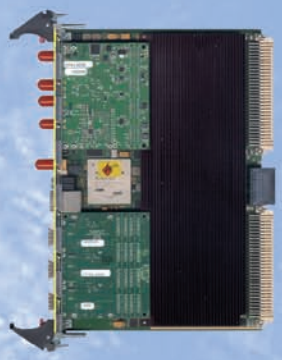

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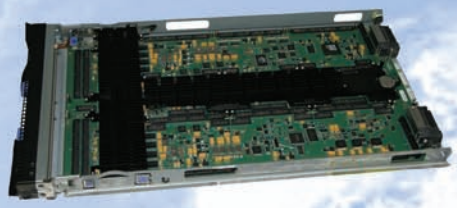

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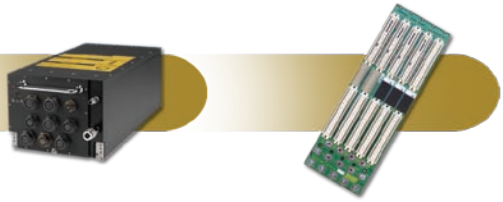


VITA News

By Ray Alderman

It is time for an optical architecture road map

At the risk of irritating all the copper-based creatures in the embedded backplane and board business, it is time for us to start thinking about optical architectures. The semiconductor folks keep upping the data transfer frequencies with every next-generation chip: The 2.5G is now old technology, 5G is being deployed, and 10G is developing rapidly. And we are heading to 100G connections in a few years. Every time the frequency goes up, the backplane folks pull their hair out trying to make it work consistently and reliably on copper. We are near the end for copper-based links running more than a few inches, so it is time to develop an optical road map.

And, as many of my readers know, I have been advocating the transition to optical architectures and hexagonal board formats in high-performance computing machines at the VSO for about four years now. Figure 1, a futuristic concept of an optically connected computing cluster, shows how both these concepts would look.

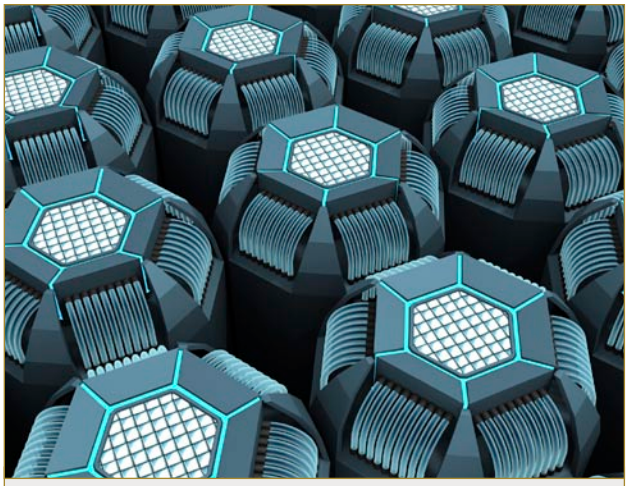


Figure 1 | A xenomorphic optically interconnected computing cluster using hexagonal boards.

An attempt at a road map

The primary way to look at optical architectures is the domain perspective: chip-to-chip, board-to-board, and box-to-box. IBM and others have been working on optical chip-to-chip interconnect technology, but it is currently in the nascent phase (see http://domino.research.ibm.com/comm/research_projects.nsf/pages/photonics.index.html). The market driving this semiconductor research and component development is the data center where bandwidth requirements rise every day. But many embedded market segments can benefit from these new opto chips aimed at data centers.

Knitting together an optical backplane

Boards are already being interconnected in backplanes using fibers. Just look at the backplane as a patch panel of holes where the fibers pass through to the connectors (see www.vita.com/vaofiles/FlexPlane.pdf). So there are many ways to interconnect boards in backplanes using fibers, with different connectors and layouts. We have already seen numerous programs implementing OpenVPX (VITA 65) boards, and they are using discrete fiber cables (with ferules) plugged into the optical connector block on the backplane defined in the VITA 66 specification.

Here is a better way

These backplane patch panels (using fiber cables) work, but they are fairly low tech. Many companies are now developing polymer reflective optical waveguides embedded in the backplane PCB material (www.springerlink.com/content/3871227217103847/fulltext.pdf). This concept holds the most promise for board-to-board optical interconnects and for the introduction of true optical backplanes in the near future. Imagine building an eight-slot mesh with fiber cable connections through a backplane [that is n(n-1) or 56 fiber cables and 112 connectors]. For a 10-board optical mesh, there are about 90 fibers and 180 connectors. As one can see, building large-scale centralized systems with optical fiber patch panel backplanes is expensive and squirrelly. Optical waveguides in the PCB material make much more sense and are cheaper and more reliable.

Optical networks between boxes

Box-to-box optical connections have been used for quite some time. These cabled connections are used heavily in the data centers now, but those applications are already moving from 10G optical Network Interface Cards (NICs) to 40G optical connections. And they want to move to 100G optical as quickly as possible. In the embedded mil/aero space, we have seen a number of optical connections used in data recorder and sensor interfaces. The components (fibers, connectors, and silicon) are mature but very slow compared to the newer developments in the data center. The increased interest in small "cubes" of electronics – Line Replaceable Units (LRUs) in Unmanned Aerial Vehicles (UAVs) and ground vehicle applications – will probably move to high-speed optical interconnections instead of copper. All distributed system interconnects will migrate to optical connections in the near future and eliminate the copper cables.

So a lot of the basics are already in place. Now the silicon engineers need to move their developments into mass production, the PCB makers need to establish a bulletproof process for embedding optical waveguides in the laminate for backplanes and daughtercards, and the connector folks need to integrate the silicon into highly reliable connectors. That should all happen in the next 18 to 24 months.

For more information, contact Ray at exec@vita.com.

VITA Standards Update

By John Rynearson

VITA 48.0, 48.1, and 48.2 recognized as American National Standards

VSO ANSI accreditation

Accredited as a Standards Development Organization (SDO) in June 1993 by the American National Standards Institute (ANSI), the VITA Standards Organization (VSO) meets every two months to address vital embedded bus and board industry standards issues. Information on ANSI/VITA standards is available on the VITA website at www.vita.com.

VSO study and working group activities

Standards within the VSO may be initiated by a study group and developed by a working group. A study group requires the sponsorship of only one VSO member. A working group requires the sponsorship of at least three VITA members.

VITA 46.4, PCI Express on the VPX Fabric Connector

Objective: To standardize the implementation of PCI Express fabric in a VITA 46 (VPX) environment and define the mapping of PCI Express links on the VPX connector.

Status: VITA 46.4 has been released by the VITA 46 working group as a VITA Draft Standard for trial use for a period of 18 months and is available from the VITA Online Store. The draft standard may be withdrawn any time before the end of the 18-month trial period and may be revised before submission to ANSI.

VITA 46.9, PMC/XMC/Ethernet Signal Mapping to 3U/6U on VPX User I/O

Objective: This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.

Status: The VITA 46 Working Group has voted to move 46.9 to ANSI ballot. Anyone with a direct and material interest in 46.9 should contact the VITA technical director at techdir@vita.com and request to be part of the 46.9 balloting group.

VITA 48.0, 48.1, 48.2

Objective: Establish a set of mechanical specifications for embedded modules.

Status: VITA 48.0, 48.1, and 48.2 have been recognized as American National Standards. Copies are available from the VITA website.

E-cast

Editor's note: *This update is based on the July 2010 VSO meeting. Additional 2010 VSO meetings are scheduled for September and November.*

Be sure to check out our online E-cast archives for the latest video and audio updates on VITA 41, 46, 48, and 65. See www.opensystemsmedia.com/ecast.

VITA 51.2, Physics of Reliability Failure

Objective: Establish uniform practices, take advantage of current developments, and clarify reliability prediction expectations using physics of failure methodologies.

Status: VITA 51.2 is currently in working group ballot. Once the ballot is completed, the draft will be revised based on comments received.

ANSI/VITA 65, OpenVPX

Objective: To provide a standard for commonly used VPX profiles.

Status: The OpenVPX working group has adopted a set of procedures for revising the document every six months as required. Proposed new profiles were reviewed at the July VSO meeting.

VITA 68, VPX Compliance Channel

Objective: Develop a compliance channel standard to ensure interoperability for embedded modules.

Status: The VITA 68 working group continues to work on defining the characteristics for channel compliance. A statement of work is also being prepared to guide upcoming simulation efforts.

VITA 71, New Generation Mezzanine

Objective: To define a new mezzanine standard for embedded modules.

Status: This effort is in the exploratory phase. The working group plans to start with a blank sheet of paper and define a mezzanine standard from the ground up, specifically designed for use in embedded modules.

For more information, e-mail John at techdir@vita.com.

PDF – *This column and the accompanying table are available at www.vmecritical.com, then click on VITA Standards.*

VITA Standards Activity Chart

JULY MEETING

Standard *Reaffirmed	Title	Status	*VME and CS* edition
ANSI/VITA 1.0 *2002	VME64 Standards	Released	
ANSI/VITA 1.1 *2003	VME64 Extensions	Released	Aug. 2004
ANSI/VITA 1.3 *2003	9U x 400 mm Format	Released	
ANSI/VITA 1.5	2eSST	Released	Feb. 2004
ANSI/VITA 1.6 *2005	Keying for Conduction-cooled VME	Released	
ANSI/VITA 1.7	Increased Connector Current Level	Released	
ANSI/VITA 3 *2002	Board Level Live Insertion	Released	
ANSI/VITA 4.0 *2002	IP Modules	Released	
ANSI/VITA 4.1 *2003	IP/I/O Mapping to VME64x	Released	
ANSI/VITA 5.1 *2004	RACEway Interlink	Released	
VITA 5.2	RACEway++	Withdrawn	Aug. 2004
ANSI/VITA 6.0 *2002	SCSA	Released	
ANSI/VITA 6.1 *2003	SCSA Extensions	Released	
ANSI/VITA 10 *2002	SKYchannel Packet Bus	Released	
ANSI/VITA 12 *2002	M-Modules	Released	
ANSI/VITA 13	Pin Assignments for HIC on VME	Withdrawn	
ANSI/VITA 17.0 *2004	Front Panel Data Port	Released	
ANSI/VITA 17.1	Serial Front Panel Data Port	Released	Feb. 2004
VITA 17.2	Serial Front Panel Data Port (SFPDP) Channel	Working Group	Dec. 2009
VITA 19.0	BusNet Overview	Withdrawn	
ANSI/VITA 19.1	BusNet MAC	Withdrawn	
ANSI/VITA 19.2	BusNet LLC	Withdrawn	
ANSI/VITA 20 *2005	Conduction-cooled PMC	Released	Apr. 2005
ANSI/VITA 23 *2004	VME64x Extensions for Physics	Released	
ANSI/VITA 25	VISION	Withdrawn	
ANSI/VITA 26 *2003	Myrinet-on-VME	Released	
ANSI/VITA 29	PC•MIP	Released	
ANSI/VITA 30.0 *2005	2 mm Connector Practice on Euroboard	Released	
ANSI/VITA 30.1	2 mm Conduction-cooled Euroboard	Released	
VITA 30.2	Power Connector Equipment Practice	Released	Apr. 2007
ANSI/VITA 31.1	GbE on VME64x Backplanes	Released	Feb. 2004
ANSI/VITA 32	Processor PMC	Released	Feb. 2004
VITA 34	A Scalable Electromechanical Architecture	Working Group	Apr. 2004
ANSI/VITA 35 *2005	Pin Assignments for PMC to VME	Released	
VITA 36	PMC I/O Modules	Withdrawn	Apr. 2004
ANSI/VITA 38	System Management on VME	Released	
ANSI/VITA 39	PCI-X Aux. Std. for PMCs and PrPMCs	Released	Feb. 2004
ANSI/VITA 40	Status Indicator	Released	Dec. 2009
ANSI/VITA 41.0	VXS: VME Switched Serial	Released	Oct. 2006
ANSI/VITA 41.1	VXS: InfiniBand Protocol Layer	Released	Oct. 2006
ANSI/VITA 41.2	VXS: RapidIO Protocol Layer	Released	Oct. 2006
VITA 41.3	VXS: GbE	Working Group	Apr. 2006
VITA 41.4	VXS: PCI Express	Working Group	Apr. 2006
ANSI/VITA 41.6	VXS: 1x GbE Control Channel Layer	Released	Sept. 2009
VITA 41.7	VXS: Processor Mesh Topology	Working Group	
VITA 41.8	VXS: 10 GbE Protocol Layer	Working Group	June 2009
VITA 41.10	VXS: Live Insertion Requirements for VITA 41 Boards	Working Group	Apr. 2006
VITA 41.11	VXS: Rear Transition Modules	Working Group	Apr. 2006
VITA 42.0	XMC	Released	Feb. 2009
ANSI/VITA 42.1	XMC: Parallel RapidIO	Released	Oct. 2006
ANSI/VITA 42.2	XMC: Serial RapidIO	Released	Oct. 2006
ANSI/VITA 42.3	XMC: PCI Express	Released	Oct. 2006
VITA 42.4	HyperTransport	Working Group	Apr. 2005
ANSI/VITA 42.6	XMC: 10 GbE 4-Lane Protocol Layer	Released	June 2009
VITA 42.10	XMC: General Purpose I/O	Working Group	

Defining Standards

VITA 71: Revolutionary mezzanine standard aims to replace PMC, XMC standards

By Dean Holman, Greg Rocco, and Dan Toohey

The VITA 71 "Rugged Mezzanine" standard will define the next-generation mezzanine cards that will allow products to be developed with electrical interfaces supporting higher-power, -speed, and -performance applications. The need for this standard has become increasingly evident in the markets that VITA serves, as requirements intensify for a standardized mezzanine solution that supports the protocols, power requirements, physical interfaces, and thermal management technologies of future mezzanine cards while optimizing system Size, Weight, and Power (SWaP). The VITA 71 Working Group comprises more than 20 companies including board, system, and connector vendors and large prime contractors.

The scope of the VITA 71 Working Group is to define a groundbreaking mezzanine standard to replace the existing PMC and XMC standards. Whereas the migration from PMC to XMC was evolutionary, VITA 71 will be revolutionary. It will begin with a clean slate rather than being burdened with support for older mezzanine standards and will deliver denser processing solutions in lower weights that can be cooled more efficiently. VITA 71 will support:

- Next-generation multi-Gigabaud signaling rates (targeting up to 12+ Gbaud)
- Convection and conduction cooling
- Module front-panel and backplane connector I/O interfaces
- User-defined I/O
- System management

VITA 71 will optimize:

- Mezzanine and carrier board real estate utilization
- Power system distribution
- Mezzanine and carrier board cooling capabilities with support for convection and conduction cooling
- Allocation of pins, leveraging OpenVPX (VITA 65) Slot Profiles experience for uses such as management and fabric connection to the carrier card and user I/O to the backplane

Currently, PMC and XMC connectors are not rated for operation at the next-generation baud rates, for example

>5 Gbaud, and they require significant real estate on the carrier and the mezzanine cards. The PMC/XMC sites do not bound power consumption beyond pin limits or provide adequate guidance or mechanisms for appropriate thermal management of the site. Additionally, the PMC/XMC sites require up to six unique voltage rails if there is a PMC/XMC site and support 3.3V_AUX as a separate rail. These and other factors – including the integration of more processing power and capabilities per square inch, and the need to locate sensor input closer to processors in smaller deployed systems – underscore the need for a revolutionary standard.

VITA 71 standard's road map

Today, rules are bent and a mezzanine/motherboard pair is often customized to optimize the pair for increased power or thermal performance, moving away from existing standards and creating interoperability challenges even for the same vendor. The VITA 71 standard will address this and deliver better interoperability between mezzanine and carrier vendors. It will provide increased interface speeds as well as thermal and power capacity, which will enable higher-speed processing capabilities on a mezzanine and higher-performance I/O in a SWaP-optimized setting.

With the VITA 71 standard, prime contractors will have the flexibility to change vendors as needed with fewer thermal and mechanical interoperability concerns, aligning with customers' goals of modeling upgrades and executing shorter design cycles.

VITA 71 progress

The VITA 71 Working Group was established last January. The first draft of the standard is expected to be complete by January 2011. Once published, it is expected that this standard will generate revisions in other VITA standards such as VITA 65, OpenVPX; VITA 46.11, VPX: System Management; and VITA 49, VITA Radio Transport (VRT).

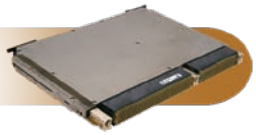
Dean Holman *is Manager of Sustaining Engineering at Mercury Computer Systems and Chairman of the VITA 71 Working Group. He can be contacted at dean@mc.com.*

Greg Rocco *is Consulting Systems Engineer in the System Architecture Group at Mercury Computer Systems. He can be contacted at rocco@mc.com.*

Dan Toohey *is a Consulting Hardware Engineer at Mercury Computer Systems. He can be contacted at dtoohey@mc.com.*

Standard *Reaffirmed	Title	Status	*VME and CS* edition
VITA 42.20	XMC: Dual Fabric I/O	Working Group	
VITA 43S	Hot Swap NextGen Mezzanine	Inactive	Feb. 2004
VITA 45S	Serial VME	Canceled	Apr. 2004
ANSI/VITA 46.0	VPX: Base Specification	Working Group	Feb. 2009
ANSI/VITA 46.1	VPX: VMEbus Signal Mapping	Working Group	Feb. 2008
VITA 46.3	VPX: Serial RapidIO on VPX Fabric Connector	Trial Use Standard	Summer 2010
VITA 46.4	PCI Express on the VPX Fabric Connector	Working Group	Fall 2010
VITA 46.5	VPX: HyperTransport	Inactive	
VITA 46.6	VPX: GbE	Working Group	Spring 2010
VITA 46.7	10 GbE on VPX	Trial Use Standard	Summer 2010
VITA 46.9	PMC/XMC/Ethernet Signal Mapping to 3U/6U on VPX User I/O	Working Group	Fall 2010
ANSI/VITA 46.10	Rear Transition Module for VPX	Released	Dec. 2009
VITA 46.11	System Management on VPX	Working Group	Spring 2010
VITA 46.12	Fiber Optic Interconnect	See VITA 66	Dec. 2009
VITA 46.14	Mixed Signal VPX	See VITA 67	Dec. 2009
VITA 46.20	VPX Switch Slot Definition	See VITA 65	June 2009
VITA 46.21	Distributed Switching on VPX	See VITA 65	June 2009
ANSI/VITA 47	Env., Design and Const., Safety, and Qual. for Plug-in Units	Released	June 2006
VITA 47r1	Revisions to ANSI/VITA 47	Released	Feb. 2008
VITA 47r2	Revisions to ANSI/VITA 47	Working Group	Dec. 2009
VITA 48.0	REDI: Ruggedized Enhanced Design Implementation	Working Group	Fall 2010
VITA 48.1	Mechanical Specs for Microcomputers Using Air Cooling	Working Group	Fall 2010
VITA 48.2	Mechanical Specs for Microcomputers Using Conduction Cooling	Working Group	Fall 2010
VITA 48.3	Mechanical Specs for Microcomputers Using Liquid Cooling	Working Group	
ANSI/VITA 49.0	VITA Radio Transport (VRT)	Released	May 2009
ANSI/VITA 49.1	VITA Radio Link Layer (VRL)	Released	May 2009
VITA 50	Best Practices for Electronic Module Cooling	Inactive	Dec. 2007
ANSI/VITA 51.0 *2008	Reliability Prediction	Released	Aug. 2008
ANSI/VITA 51.1 *2008	Reliability Prediction: MIL-HDBK-217 Daughter	Released	
VITA 51.2	Physics of Reliability Failure	Working Group	Fall 2010
ANSI/VITA 51.3	Qualification and Environmental Stress Screening	Released	Spring 2010
VITA 52	Lead-free Practices	Working Group	Oct. 2006
ANSI/VITA 53	Commercial Technology Market Surveillance	Released	Summer 2010
VITA 54	Embedded Platform Management Architecture (EPMA)	Inactive	Aug. 2005
VITA 55	Virtual Streaming Protocol	Inactive	Feb. 2009
VITA 56	Express Mezzanine Card (EMC)	Inactive	Oct. 2007
ANSI/VITA 57 *2008	FMC: FPGA Mezzanine Card	Released	Feb. 2009
VITA 57.1	FPGA I/O Mezzanine Pin Assignments	Working Group	June 2009
ANSI/VITA 58.0	Line Replaceable Integrated Electronics Chassis	Released	May 2009
VITA 59	RSE: Rugged System-on-Module Express	Working Group	Dec. 2008
VITA 60	Alternative Connector on VPX	Working Group	Dec. 2009
VITA 61	Alternative Connector for XMC	Working Group	Dec. 2009
VITA 62	Power Supply Modules	Working Group	Dec. 2009
VITA 63	KVPX	Working Group	Feb. 2009
VITA 64	Optimized Footprint for VITA 60	Working Group	Feb. 2009
ANSI/VITA 65	OpenVPX	Released	Fall 2010
VITA 66	Fiber Optic Interconnect (Formerly 46.12)	Working Group	Spring 2010
VITA 67	Analog/RF Interconnect (Formerly 46.14)	Working Group	Spring 2010
VITA 68	VPX Compliance Channel	Working Group	Fall 2010
VITA 69	Common Glossary	Working Group	
VITA 70	Common Standard Template	Working Group	
VITA 71	New Generation Mezzanine	Working Group	Fall 2010
VITA 72	Connector Comparision Testing	Working Group	
VITA 73	Small Form Factor-v73	Working Group	Summer 2010
VITA 74	Small Form Factor-v74	Working Group	Summer 2010

For corrections or suggestions, contact Chris Ciufo, *VME and Critical Systems* magazine, at cciufo@opensystemsmedia.com.



By Ron Huizen

OPENVPX INTERCONNECTS...

Reconfigurable boards ease OpenVPX's protocol and interconnect challenges

OpenVPX's (VITA 65's) primary goal is to increase interoperability for VPX (VITA 46) technologies. And while OpenVPX is certainly a large step in the right direction, the many differing requirements across various applications make it impossible to standardize on a single high-speed serial protocol and associated interconnect topology. However, by providing for adaptable I/O, a reconfigurable OpenVPX board can allow system designers to explore different protocols and topologies – and mix and match them – providing a flexible interface to the rest of the system.

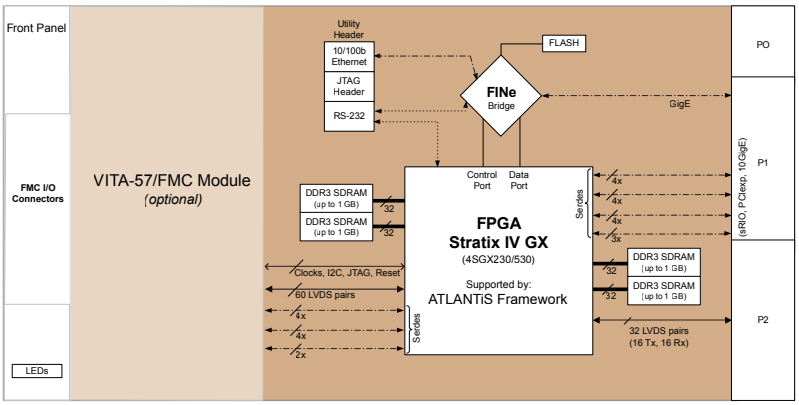


Figure 1 | BittWare S4-3X-VPX reconfigurable VPX/OpenVPX board

So many protocols, so little time

While initial versions of VME were standardized, as bandwidth needs grew, special secondary buses and data paths were added, often relegating the VMEbus to a simple control plane. High-speed switched serial protocols attempt to satisfy both the bandwidth needs of the data plane and the connectivity needs of the control plane, but the problem of too many different available protocols remains. There were hopes that the user community would eventually settle on one, but instead there are now three dominant protocols – PCI Express, Serial RapidIO, and 10 GbE – each with its own strengths and heritage.

While PCI Express provides ease of use from a software and system point of view, Serial RapidIO can't be beat for data throughput and low latency. And 10 GbE is a natural fit in a networking-based application. All of these switch fabric protocols typically assume a backplane topology where each board is connected to a switch, and hence can access any other board in the system. These topologies can be single or dual star, with redundant switch slots.

While the switch fabrics and switched backplanes provide flexibility, they do come at a cost, both for the switch board itself and in terms of resources on each board for running the protocol. If all the application really needs is pure board-to-board data flows, the lightweight protocols – including SerialLite and Aurora – are perfect when combined with a point-to-point backplane topology like a ring. These lightweight protocols provide high throughput and low resource usage by not requiring the overhead of switched protocols.

Amidst so many switch fabrics and protocols, OpenVPX provides some help in figuring this all out by defining standard backplane and slot profiles covering the major topologies. But OpenVPX does not dictate one particular high-speed serial protocol or interconnect topology, instead enabling them all. This is where a reconfigurable OpenVPX board can truly provide a remedy.

Reconfigurable OpenVPX boards to the rescue

A reconfigurable OpenVPX board uses FPGA technology to allow adaptation to virtually any OpenVPX backplane, and hence system. With the ability to run any of the serial protocols – including PCI Express, Serial RapidIO, and 10 GbE, as well as the lightweight point-to-point protocols – a reconfigurable OpenVPX board can make use of the protocol that best fits the application. These boards can also be used to create systems that utilize multiple protocols, acting as a bridge between them. To get the best of both worlds, backplane topologies can even be mixed, for example combining a single switched fat pipe with a ring of board-to-board fat pipes. Along with the multi-gigabit interfaces, a reconfigurable OpenVPX board should also provide standard I/O, such as LVDS, to enable interfacing to other parts of the system. Besides direct backplane connections, a great way to do this is with a VITA 57 FPGA Mezzanine Card (FMC), which can provide tremendous system flexibility. With multi-gigabit transceivers and LVDS connected to both the VPX backplane and an FMC site, such an OpenVPX board can be easily adapted to meet system-interfacing needs.

A reconfigurable OpenVPX board is shown in Figure 1. This board has 15 multi-gigabit serial connections to the OpenVPX backplane and 10 to the VITA 57 FMC site. A single Ethernet interface is used for board control and setup, including reconfiguring the FPGA and burning FPGA images into the flash. With multiple FPGA images stored, these boards can be reconfigured with a simple command over Ethernet to match numerous OpenVPX profiles.

Ron Huizen, *VP of Technology at BittWare, Inc., can be contacted at rhuizen@bittware.com.*

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Implementing system management in OpenVPX

By Mark Overgaard

The high-energy campaign to complete the OpenVPX standard has been complemented by a parallel effort to define a generic system management layer for use in OpenVPX and other VPX systems. The resulting VITA 46.11 architecture and corresponding implementation considerations are presented.

System management in OpenVPX (VITA 65) refers to the combination of software, hardware, and firmware responsible for administrative tasks associated with maintaining an OpenVPX system. Such functions include sensor monitoring, hardware inventory management, and firmware installation/upgrades. Historically, this set of functions, which is present in some form within any substantial VME-based system, has been implemented as part of the application layer. There has not been a distinct, VITA-architecture-defined layer that handles it.

With increased emphasis on interoperability, reduced integration effort, and time-to-market in the OpenVPX initiative, this layer needs to be architected and specified so that system integrators can combine platform elements for their applications as quickly and efficiently as possible, while implementing the level of such management that is suitable for their applications.

These challenges are being addressed within the VITA Standards Organization (VSO) through development of VITA 46.11, the System Management on VPX standard, which is currently in the early draft state. OpenVPX allocates pins in backplane slots and on modules for system management connections and mandates VITA 46.11 compliance on those pins if they are used. VITA 46.11 can be applied to any compatible VPX-based architecture.

The following discussion introduces the VITA 46.11 architecture, including the levels of management and the tiers within those levels that it defines. Possible approaches to implementing VITA 46.11 at the module level are also presented.

Levels of management for OpenVPX in VITA 46.11

VITA 46.11 identifies three levels of management: module, chassis, and system. At the module level, an Intelligent Platform Management Controller (IPMC) handles the local module management responsibilities, representing that module to the Chassis Manager. Using an I^2C-based Intelligent Platform Management Bus (IPMB) link, the Chassis Manager monitors the collection of modules in a chassis and represents the entire chassis to a System Manager. The System Manager is a logical entity that is typically linked to the Chassis Manager via some higher-speed connection such as Ethernet; it monitors and supervises the operation of one or more chassis that combine to form an OpenVPX-based system.

VITA 46.11 defines the responsibilities and interfaces of the IPMC and Chassis Manager blocks, but defers definition of the System Manager to the application. Figure 1 shows this architecture with two example IPMC-equipped modules and the Chassis Manager monitoring them.

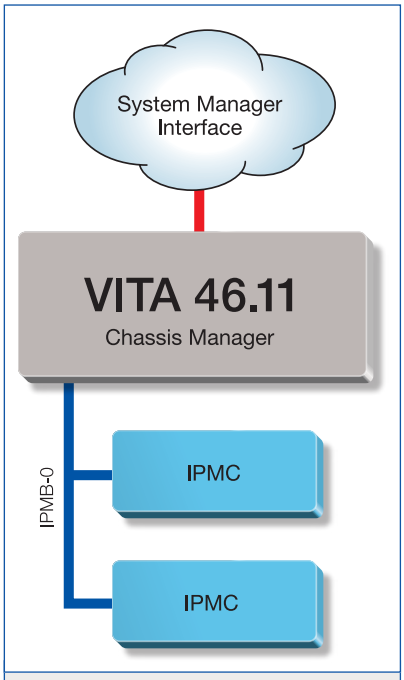

Figure 1 | Overall architecture for VITA 46.11 system management

Here is a simple example of how the VITA 46.11 facilities could contribute to the operation of a real OpenVPX system. Each OpenVPX module in the system would have one or more temperature sensors, perhaps monitoring key temperature-sensitive sites on that module. For each of those sensors, the module developer or system integrator would define temperature thresholds of increasing severity for higher temperatures, based on the temperature operating profile for the device(s) at a given site on the module. Any temperature measurement that crosses one of those thresholds would trigger an event message to the Chassis Manager. By monitoring and integrating such event messages, the Chassis Manager could identify the need to change the speed of the fan(s) for all or a subset of the modules in the chassis, for instance, and monitor the effects of such changes on the temperatures in the chassis.

Like AdvancedTCA, VITA 46.11 leverages the Intelligent Platform Management Interface (IPMI), which is widely used in the PC and server industry for hardware platform management facilities. For example, IPMI provides a rich infrastructure for defining and monitoring analog and digital sensors in an implementation-independent and consistent way. These facilities allow independently implemented elements of an OpenVPX system from different suppliers (including chassis vendors,

module vendors, and system integrators, for instance) to be monitored by a single Chassis Manager that has a unified view of the state of the chassis and all the analog and digital sensors that its elements include.

Functional tiers provide architectural flexibility

One challenge for VITA 46.11 system management is to provide the appropriate extent of these services to fit the needs of a given application. Different applications and different system integrators can have very different views regarding the partitioning of management functions between application layers and underlying infrastructure layers. VITA 46.11 addresses these challenges by defining functionality tiers for both the IPMC and the Chassis Manager: tentatively three tiers for each level. This approach allows chassis and module suppliers, as well as their customers, to choose the appropriate tier level for the management infrastructure layer, while still gaining the interoperability and cost effectiveness that result from standardization.

For instance, the tier 1 IPMC provides minimal management functionality, such as inventory data and a few simple sensors, but is designed to interoperate successfully on a module in a chassis with other modules that include more sophisticated (higher tier) IPMCs and a Chassis Manager. Furthermore, the tier 1 IPMC is being defined so that it can be implemented with no firmware at all – potentially just with logic in a flash-based FPGA, for instance.

A tier 1 IPMC could be a good choice for a simple module or for a module where avoiding firmware might simplify formal certification. Alternatively, modules with tier 1 IPMCs might be chosen by a system integrator who decides that the great majority of the system management layer should be implemented as part of the application, not by an underlying infrastructure.

Tier 1 IPMCs have disadvantages, however. For instance, their support for analog and digital sensors is severely restricted: As currently planned, tier 1 IPMCs will support only a handful of simple sensors, and the Chassis Manager will have to poll every one of those sensors to get updates on state changes. Higher-tier IPMCs will have full-function sensor capabilities (among other substantial benefits), enabling much more effective operation of the platform management layer.

Leveraging AdvancedTCA's hardware platform management layer

Another key decision in the VITA 46.11 initiative has been to leverage the widely used hardware platform management layer in PICMG's proven AdvancedTCA framework. This decision allows the OpenVPX community to take advantage of AdvancedTCA's years of specification development and field experience, while still adapting the AdvancedTCA management architecture to the different needs and constraints that characterize OpenVPX applications. For instance, OpenVPX modules, by architectural choice, are not hot-swappable in a live system, which allows considerable simplifications in the system management architecture.

Adapting the AdvancedTCA management architecture for the OpenVPX context yields a second benefit as well: minimizing the needed investments for OpenVPX vendors who also develop products in the AdvancedTCA form factor. Such vendors can potentially spread the benefits of management investments across both communities.

Implementation options for IPMC on an OpenVPX module

One way to implement a VITA 46.11 management controller, especially a higher-tier IPMC (that is, above tier 1), is with a generic microcontroller. The CPU in such a device implements the controller firmware and uses the available integrated peripherals (such as voltage and temperature monitors) to provide key management data.

If the microcontroller includes an Ethernet port, it can potentially connect with in-chassis Ethernet, such as an OpenVPX Control Plane, for substantial performance benefits in IPMC firmware upgrades and other operations.

Another way to implement a full-function VITA 46.11 IPMC is with an intelligent mixed signal FPGA, such as Actel's SmartFusion device. The microcontroller and analog subsystems of such an FPGA implement the IPMC firmware and analog sensors, possibly with significantly more capabilities in the analog area; the 10/100 Mbps Ethernet interface can implement a LAN connection. Figure 2 provides a high-level block diagram of an example VITA 46.11 full-function IPMC based on an intelligent mixed signal FPGA.

The FPGA fabric in such an IPMC adds customizability, both for management architecture additions – such as an IPMI-defined interface between the IPMC and a main processor on the module or extra I^2C ports – and for board-specific logic that might otherwise require a separate programmable logic device.

Implementing an example VITA 46.11 IPMC

Creating a compliant and interoperable VITA 46.11 IPMC is no small project, however. One challenge is that the standard itself is not yet complete. In addition, the specifications leveraged by VITA 46.11 (such as AdvancedTCA hardware platform management and IPMI) encompass more than 1,000 pages of management-focused specification content. Most OpenVPX module developers who want to support VITA 46.11 choose to use an existing management controller implementation, such as one from the Pigeon Point Board Management Reference (BMR) family. If the existing controller supports the requirements of an AdvancedTCA IPMC, the likelihood

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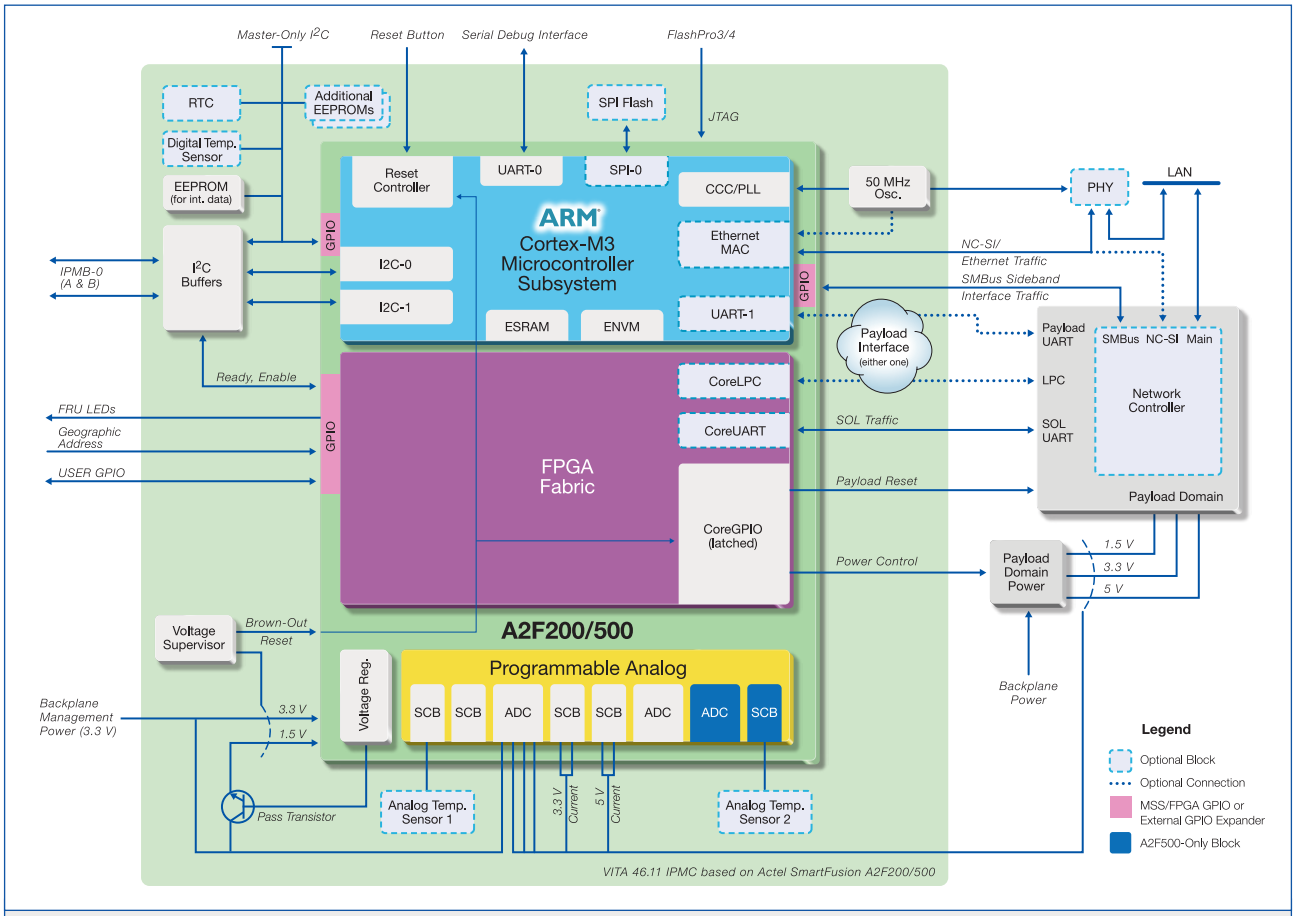

Figure 2 | Example VITA 46.11 IPMC based on a SmartFusion intelligent mixed signal FPGA

is high that it can support VITA 46.11 IPMC requirements with some level of firmware updates once the VITA 46.11 standard is finalized.

In addition to the normal management functions implemented by the microcontroller and analog and FPGA subsystems of the example intelligent mixed signal FPGA, this IPMC can implement advanced facilities based on a connection with a network controller that is part of the payload domain of the module (that is, the portion of the module not focused on system management). Through a connection to an Ethernet-based OpenVPX Control Plane, for instance, such an IPMC can support the following:

- Serial Over LAN (SOL): Access via a Control Plane LAN to serial ports that are either on the IPMC or on the major processor(s) implemented on the module: Such LAN-based serial port access can be a big benefit compared to attaching physical serial cables to every serial port of interest in a system.
- Upgrading IPMC firmware or IPMC-accessible programmable logic devices via LAN: For modules and systems that implement such upgrades, using a LAN connection can yield 15x or more speedups, compared to doing them via the IPMB links.

System management for OpenVPX is catching on

The benefits of a system management layer for OpenVPX are gaining increasingly wide recognition. Adopting a proven management solution for that subsystem of an OpenVPX module can save time and money and preserve scarce development resources for value-added functionality of the module. With careful implementation choices, VITA 46.11-based system management for OpenVPX can deliver a standardized implementation of the hardware platform management layer that saves development and integration time, plus offers improved interoperability. This layer also preserves the flexibility for system developers and integrators to decide how to partition the system management function between the standardized layer and their application subsystems. **CS**

Mark Overgaard *is founder and President of Pigeon Point Systems (PPS), now an Actel company. Mark is a leader in PICMG technical subcommittees, including those addressing hardware platform management of AdvancedTCA, AdvancedMC, and MicroTCA. He also actively participates in the VITA 46.11 working group. Prior to founding PPS in 1997, Mark was VP, Engineering at Lynx Real-Time Systems and TeleSoft. He can be contacted at mark@pigeonpoint.com.*

Pigeon Point Systems
831-438-1565
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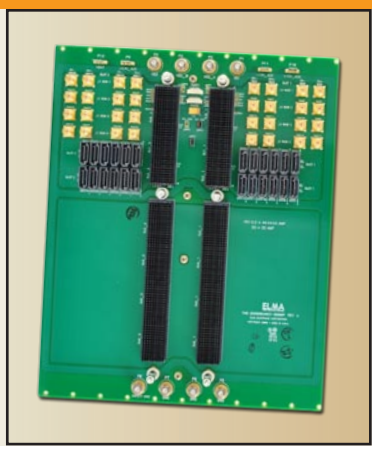
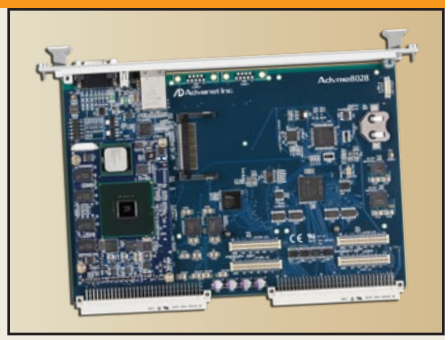
Test backplane for VPX boards



The 2-slot Test Backplane renders convenient VPX board testing. Designed to the latest VITA 46.0 VPX specifications, it accepts 6U cards and 3U is supported by use of a shelf divider. A wider slot pitch allows more space for attaching to probes. The J1 "A" channel is broken out to 16 SMA connectors for each slot (32 total), and J1 "B," "C," and "D" channels are each broken out to 4 SATA II cable headers for a total of 12 headers per slot (24 total). The test backplane allows simultaneous access of J1 fabric signals with a standard VPX RTM module for J2-J6 signals. And more than 2 VPX modules may be interconnected by using additional 2-slot test backplanes.

www.elma.com **ELMA BUSTRONIC**

Atom-based VME board



The EUROTECH Advme8028 Atom 6U VME board is ideally suited for rugged, mobile applications requiring exceptionally low power. Specifically, the board utilizes the Intel Atom processor Z500 series at 1.1, 1.33, or 1.6 GHz, in addition to onboard DDR2-533 SDRAM (512 MB or 1 GB). Accoutrements include front-panel GbE, a CompactFlash slot, 2x 32-bit/33MHz PMC slot, VGA and USB connectors, plus two optional COM ports. The board is available in a range of versions sporting multiple CPU clock frequencies and memory sizes. Operating temperatures range from 0 °C to +70 °C or -40 °C to +85 °C. Multiple operating systems, such as Win7, Windows XPe, VxWorks, and Linux, are supported.

www.eurotech-inc.com **EUROTECH**

VPX development system

The DEV-4200 VPX development system for 3U boards provides a capability of configuring up to an 8-slot system that supports any mix of 3U convection- or conduction-cooled boards, in addition to 3U transition modules on .8" or 1.0" centers. Backplane profiles and topologies are or will be available to test any board configuration, and power-supply choices support 12 H- and 5 VH-based systems. Optional "VEN" power systems are available for cost savings if desired. Cooling is delivered equally at each slot with up to 700 LFM across the boards with no dead spots. Chassis side panels are removable for side-board access and probing. Airflow through the board area affords adequate cooling for even high-power boards, and legacy wedge-lock or VITA 48.2-style card guides are available as an option.

www.dawnvme.com
DAWN VME PRODUCTS, INC.

VPX/CompactPCI 1/2 ATR chassis

The XPand4200 is a 1/2 ATR forced-air-cooled chassis featuring reduced height and length for conduction-cooled modules. It features forced-air-cooled sidewall heat exchangers and supports increased cooling through an external cold plate. Physical dimensions are 4.88" (W), 6.0" (H), and 13.5" (L) without the removable memory module attachment. Meanwhile, the chassis footprint is 4.88" (W) x 9.6" (L). Six slots support conduction-cooled 3U VPX, 3U CompactPCI, or power supply modules, and 3U VPX and CompactPCI backplanes are available. The chassis has configurable front-panel I/O connectors and an optional removable memory module attachment and consumes up to 200 W from a MIL-STD-704 28 VDC or 115 VAC source.

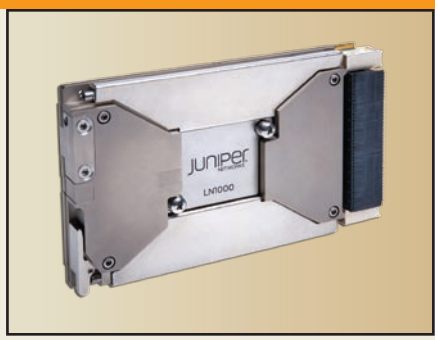
www.xes-inc.com
EXTREME ENGINEERING SOLUTIONS

Atom-based SBC

General Micro Systems, Inc.'s Atom XPC40x is a new rugged, Intel Atom-based, conduction-cooled SBC. Powered by a high-performance 1.6 GHz Intel Atom processor with 512 KB of L2 cache, the SBC is about the size of an iPhone and delivers high performance and ultra-low power consumption: 10 W max, 3 W typical. It is ultra-lightweight at less than three-tenths of a pound, and has an ultra-small footprint: 2.5" x 3.3" x 0.5". It is available in a conduction-cooled version (-40 °C to +85 °C) or a standard version (0 °C to +60 °C).

www.gms4sbc.com
GENERAL MICRO SYSTEMS, INC.

VPX mobile secure router



The LN1000 is a VPX mobile secure router used in the U.S. Army's Warfighter Information Network-Tactical (WIN-T) program, now available for use in industries such as defense, public safety, utilities/energy, smart grid, and others. The router, which measures 4" x 6" x .85" and weighs 1.5 lbs, provides transmission of data, video, and audio traffic for data aggregation, surveillance, or communications applications. It securely interconnects platforms such as remote monitoring or sensor stations, UAVs, and so forth to their operations centers or central command. It offers high performance with low power consumption of 35 W. LN1000 operates at -40 °C to +85 °C, and a conduction-cooled design eliminates the need for external power. Notably, the router can be deployed onto existing platforms.

www.juniper.net **JUNIPER NETWORKS, INC.**

Non-blocking OpenVPX GbE switch

The VX3910 is a high-end OpenVPX non-blocking GbE switch. It allows for flexible implementation of network-centric situational awareness and High Performance Embedded Computing (HPEC) applications in markets that include military, medical, and energy. It is also highly suitable for autonomous systems such as UAVs and AUVs. The switch is a fully managed L2 solution (L3 upgradable) with a total of 28 GbE ports. VX3910 has quad 1000BASE-T uplinks on the front panel, with 2 reroutable on the backplane, in addition to a 10/100/1000BASE-T management port. It also provides Enterprise Class switching functions and is available in standard air- and rugged conduction-cooled versions.

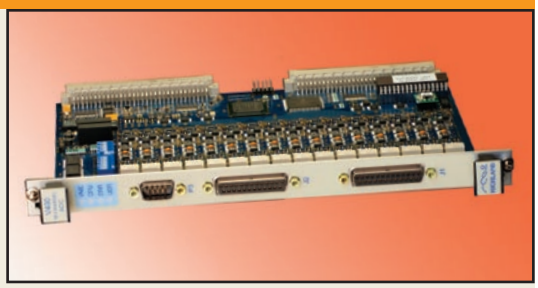
www.kontron.com **KONTRON**

SATA interface, conduction-cooled VME module

Phoenix International's VC1-250-SSD is a SATA interface, conduction-cooled VME module. The 6U, single-slot module houses one or two each 2.5" SATA Solid State Disks (SSDs) of up to 256 GB per device. The high-speed module will sustain R/W data rates of 220 MBps with an access time of 0.5 msec. It has low power consumption rates and integrated SLC NAND flash. VC1-250-SSD features an operating temperature range from -40 °C to 85 °C and functions at an altitude greater than 80,000 feet. It also withstands 50 *g*, 11 ms operational shock and 16 *g* rms, 10-2,000 Hz random vibration. VC1-250-SSD additionally meets military and IRIG 106-07 declassification standards and provides individual point-to-point device connectivity.

www.phenxint.com **PHOENIX INTERNATIONAL**

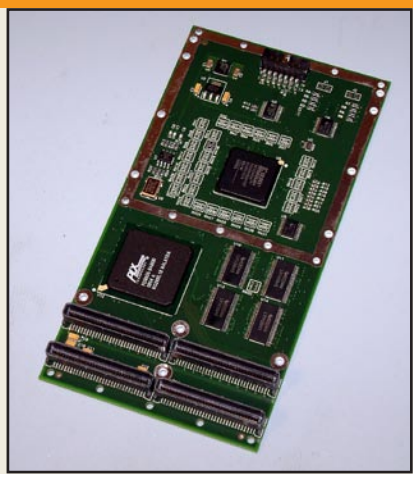
VME-based analog signal digitizer



Highland Technology, Inc.'s V490 analog signal digitizer is one in a series of high-precision VME data acquisition modules. V490 features 16 channels of independently programmable differential analog input acquisition, and input is ±10.24 mV to ±40.96 V with 16-bit resolution. Common-mode rejection is 120dB typical, with a ±10 V common-mode range. The digitizer is overload protected to ±250 V on all ranges, with a sample rate up to 500 Ksps per channel. DSP filter modes range from 1 Hz to 200 KHz, and real-time and FIFO-buffered data are supported. V490 also includes handshake-free dual-port memory, in-crate calibration check via a dedicated test connector, and a DIPswitch-set VME address with no jumpers, headers, or trimpots. BIST is optionally provided.

www.highlandtechnology.com **HIGHLAND TECHNOLOGY, INC.**

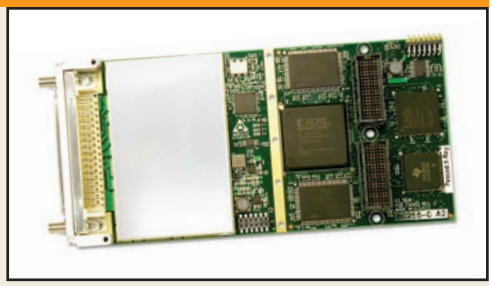
Rugged conduction-cooled PMC



Sterling Electronic Design's PMC DIO 64 is a rugged conduction-cooled PMC with 64 TTL I/O channels. It is configurable for 33 or 66 MHz and 32- or 64-bit PCI. With all 64 I/O channels and more than 95 percent of PCI signals utilized, the PMC DIO 64 is an ideal test asset for PMC host sites. The PMC includes eight 8-bit banks, with each bank selectable as input/output and 1 bank configurable as ground. Also included are 8 KB SRAM and PCI and DIO tolerance for 3.3 V or 5 V operation. Additional notables include an extended temperature range, PCI I/O voltage detection, rear I/O, and a VxWorks driver.

www.sterlingelectronicdesign.com
STERLING ELECTRONIC DESIGN

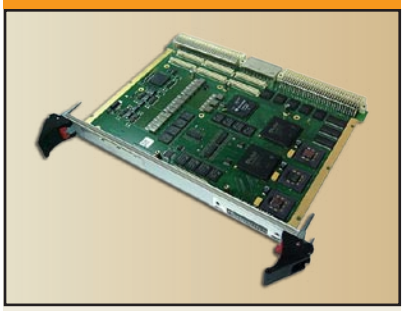
PCI Express XMC I/O module



Innovative Integration's X3-SD16 is a PCI Express XMC I/O module featuring sixteen 144 KHz, 24-bit A/D channels; sixteen 192 KHz, 24-bit DAC channels; 15.8-bit ENOB; and 110 dB SFDR A/Ds. Also included are differential instrumentation inputs with programmable 2, 10, and 20 V ranges, in addition to a ±10 V output range. The module is DC coupled for instrumentation applications and performs via a Xilinx Spartan-3A DSP 1.8 M or 3.4 M FPGA and 4 MB SRAM. X3-SD16 has a programmable or external sample clock, along with synchronized system sampling using a common reference clock, triggers, and sync.

www.innovative-dsp.com **INNOVATIVE INTEGRATION**

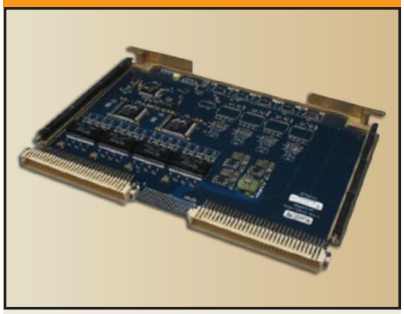
Triple-redundant 6U VME64 SBC



The A602 is a triple-redundant 6U VME64 SBC, developed according to DO-254 especially for plane (up to DAL-A) or train (up to SIL 4) applications. The SBC features a lock-step architecture and has 3x redundant PowerPC 750 at up to 900 MHz. Also included is 3x redundant 512 MB DDR RAM; 2x redundant 256 MB flash, ECC; and 1x 1 MB FRAM, ECC. It also has redundant local PSUs and a 1x standard PMC slot in addition to a 1x PMC slot for AFDX PMC (rear I/O only). Also proffered are 1x RS-232 via front and rear I/O and PMC I/O. Operating temperature is -40 °C to +50 °C with qualified components.

www.menmicro.com
MEN MICRO ELEKTRONIK GMBH

VME Ethernet switch



The COM-8000 is a 6U conduction-cooled VME Ethernet switch. It is a non-blocking, Layer 2 unmanaged Ethernet switch with auto-MDI/MDIX, autonegotiation, and speed autosensing. It features 16x 10/100 Fast Ethernet (VMEbus P2 connector) and optional 2x 10/100/1000 GbE front-panel RJ-45 or locking Molex connectors. It provides extended-temperature operation of -40 °C to +85 °C and is designed to meet MIL-STD-810G environmentals for thermal, shock, and vibration for the Jet-Helo profile. It also has RFC 2460 IP protocol support for IPv4 and IPv6 addressing.

www.parvus.com
PARVUS CORPORATION

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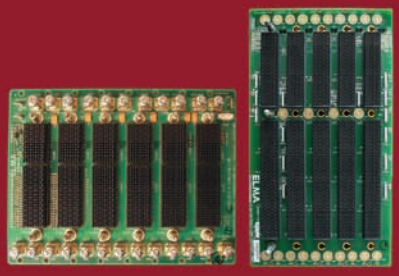
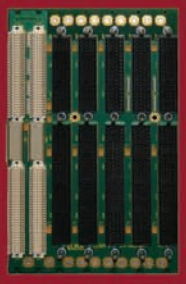
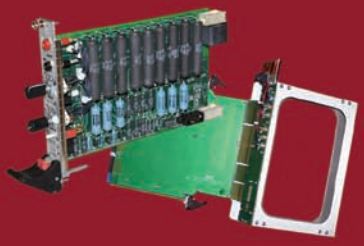


OpenVPX Backplanes



OpenVPX
Hybrid Backplanes



VPX Load Board &
Extender Board

VPX SerDes Test Modules,
RTMs & Air Baffles

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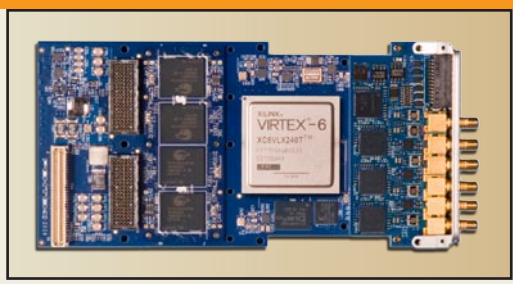
Virtex-6 data acquisition XMC module



Pentek, Inc.'s Model 71660 is a Virtex-6 FPGA Cobalt quad-channel data acquisition and processing XMC (VITA 42.0) module. It has four 200 MSps, 16-bit data acquisition channels that deliver nearly 90 dB of spurious free dynamic range, enabling users to detect small signals of interest. It is designed as a radar and software radio interface and supports Xilinx Virtex-6 LXT and SXT FPGAs. The module has LVDS connections to the Virtex-6 FPGA for custom I/O and provides up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM plus sample clock synchronization to an external system reference. Model 71660 Cobalt also proffers LVPECL clock/sync bus for multimodule synchronization, along with PCI Express (Gen 1 and 2) interfacing up to x8 wide. It is additionally offered in a conduction-cooled version.

www.pentek.com **PENTEK, INC.**

3U DC/DC converter for airborne apps

The "Power Supply: 3U DC-DC Converter" by HDL Research Lab, Inc. is designed for U.S. military airborne applications. It uses "proven low-risk" circuits that can easily be modified for other applications. Because it is designed for airborne applications, the rail-cooled power module features true N+1 capability. The converter provides high power (200 W) and features multi-output (4) [5 V, 3.3 V, ±12 V]. The 3U PICMG-compliant converter is startup sequenced and includes embedded DSP/BITE and a temperature sensor, in addition to serial interfacing and output voltage adjustable remote sense circuits. Operating temp is -54 °C to + 85 °C, and the 6.57" (L) x 3.937" (W) x 0.97" (H), <1.2 lb converter meets MIL-STD-461 and MIL-STD-704.

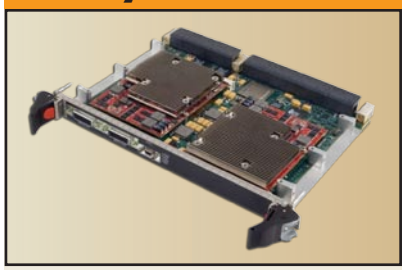
www.HDL.CC **HDL RESEARCH LAB, INC.**

Dual-Virtex-4 PMC/XMC digitizer

The AD484 is a quad-channel dual-Virtex-4 PMC/XMC digitizer. It has four A/D channels and a 10 MHz to 125 MHz sampling range, plus 14-bit data resolution. Also provided are custom clock and trigger inputs via external connectors, as is onboard clock generation in steps of 0.5 MHz. The digitizer performs high-speed DSP processing via two Xilinx Virtex-4 FPGAs (XC4VSX55, XC4VLX40, XC4VLX60, XC4VLX80, XC4VLX100, and XC4VLX160; or XC4VFX20 or XC4VFX60 with an embedded PowerPC RISC processor). Off-the-shelf IP cores are proffered, and FPGA firmware design services are available upon request. Meanwhile, AD484 has 2x 32M x 16 DDR2 SDRAM (128 MB), 4x 2M x 32 QDR2 SRAM devices (32 MB), and a 128 Mb flash device. 4x 2.5 Gbps optical transceivers for SFPDP, Fibre Channel, GbE, and InfiniBand applications are additionally included.

www.4dsp.com **4DSP**

OpenVPX ISR subsystem



Mercury Computer Systems, Inc.'s OpenVPX ISR subsystem executes Processing, Exploitation, and Dissemination (PED) within the ISR realm. It is a "high-end" image- and signal-processing subsystem for heightening warfighters' situational awareness and providing parallel data stream computing capabilities. The subsystem includes Mercury's Ensemble 6000 Series GSC6200 OpenVPX-based GPU processing module. This GPU incorporation renders SWaP advantages, and the MxM GPU form factor expedites ATI or NVIDIA GPU integration or upgrades. Additionally, the OpenVPX ISR subsystem uses open standards-based APIs, simplifying the process of mixing and matching with other technologies.

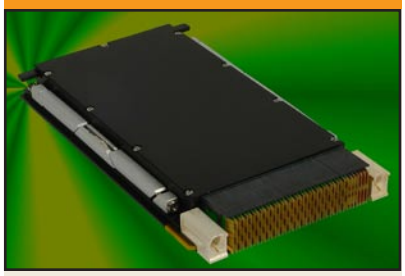
www.mc.com
MERCURY COMPUTER SYSTEMS, INC.

6U VME/VPX 3/4 ATR chassis

The High Performance 3/4 ATR Chassis from CM Computer is a sealed, contaminant-free enclosure incorporating six air-to-air heat exchangers (SixHex series). The MIL-STD-810F and MIL-STD-461E chassis has 7 universal slots for VME, VPX, and CompactPCI conduction-cooled or air-cooled 6U boards, along with thermal characteristics up to 150 W per slot. It is a single, stand-alone, low-weight solution at 13 kg and includes an integrated Temperature Supervisory Unit (TSU). An 800 W PSU accepts all military standard input voltages, and easily customizable front panel and flexible top and bottom I/O wiring is provided.

www.cmcomputer.com
CM COMPUTER

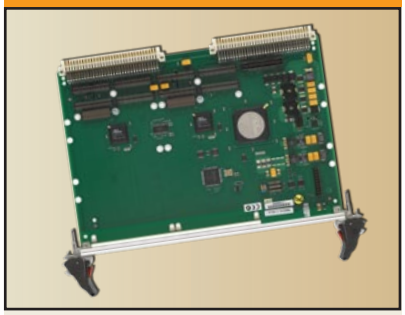
OpenVPX/ VPX-REDI SBC



Concurrent Technologies, Inc.'s TR 501/36x is an OpenVPX-compliant 3U VPX-REDI single board computer based on a 1.86 GHz Intel Core 2 Duo SL9400 processor. It is designed to VPX-REDI Type 1 Two Level Maintenance (an 0.85" pitch unit – VITA 48.2). The SBC also comprises the Intel GS45 graphics memory controller hub and Intel ICH9M-E I/O controller hub, in addition to up to 8 GB DDR3-1066 soldered SDRAM. An XMC site supports an x4 PCI Express link and Pn6 XMC rear I/O. The SBC also has OpenVPX slot profiles from 8 x1 PCIe ports through to a 1 x8 PCIe port.

www.cct.co.uk
CONCURRENT TECHNOLOGIES, INC.

6U VME expansion module



The XMCspan expansion module from Emerson Network Power Embedded Computing provides a flexible, scalable expansion framework compatible with the newest Emerson VMEbus single board computers. The module is available in a single-slot 6U VMEbus format. It includes a PLX PEX8533 PCI Express 6-port switch and Tundra Tsi384 PCI Express to PCI-X interface bridges. Support for two single-wide or one double-wide XMC or PMC is also proffered, as are stacking capability and front-panel I/O.

www.emersonnetworkpower.com/embeddedcomputing
EMERSON NETWORK POWER EMBEDDED COMPUTING

VME/VXS microwave tuner

The SI-9155 is an open-architecture, high-performance 6U VME/VXS microwave tuner used for multi-function SIGINT, COMINT, or FISINT surveillance and monitoring operations. The single-slot microwave tuner supports a frequency range of 250 MHz to 24.5 GHz and provides low phase noise, high dynamic range, and fast tuning. It supports multiple bandwidths – 1 GHz, 500 MHz, and 100 MHz – and is capable of independent or coherent operation. Other highlights include 50 W of power maximum, a weight of 4 lbs, high signal fidelity, and conduction- or air-convection-cooled versions.

www.drs-ss.com **DRS SIGNAL SOLUTIONS, INC.**

Rugged power supply for VME, VPX, and CompactPCI

Aitech Defense Systems' P230 is a rugged 3U, conduction-cooled, high-efficiency power supply measuring 3.93" high x 6.60" deep x 1.14" wide (100 mm x 168 mm x 29 mm) and weighing less than 1.65 lbs (750 g). It operates over a continuous input voltage range of 18 to 36 VDC and provides isolated voltage levels of +3.3 V, +5 V, +12 V, and -12 V at up to 10 A, 20 A, 9 A, and 1 A, respectively, or a combined total power capacity output of up to 150 W, with an efficiency of better than 85 percent. P230 is ideal for use in rugged VME-, CompactPCI-, and VPX-based subsystems. Rugged models are rated for -40 °C to +71 °C, and the power supply complies with MIL-STD-461, MIL-STD-1275, MIL-STD-704, and MIL-STD-810E.

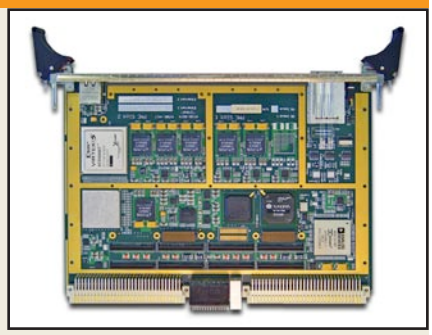
www.rugged.com **AITECH DEFENSE SYSTEMS**

Virtex-6-based reconfigurable design platform

Alpha Data's ADM-XRC-6TL is a Xilinx Virtex-6 FPGA-based reconfigurable design platform on a VITA 42.3 (PCI Express) XMC card form factor. It features a flexible board architecture that supports the larger Xilinx Virtex-6 devices, including the LX240T, LX365T, LX550T, SX315T, and SX475T. The platform is supplied with 1 or 2 GB of DDR3 SDRAM supporting transfer rates of up to 3.2 GBps and arranged in 4 independent banks for maximum flexibility. It also has up to 146 LVCMOS/LVDS I/O and 8 high-speed serial links to the front connectors. Meanwhile, 12 high-speed serial links, an x4 PCI Express I/F and 24 General Purpose IO (GPIO) are provided as standard to the rear connectors. Application-specific I/O options are available via a comprehensive range of front-panel adapter products, including LVDS, high-performance analog, Cameralink, and optical and copper RocketIO.

www.alpha-data.com **ALPHA DATA**

FPGA/PowerPC VXS multiprocessor



Nallatech's VXS-620 is an FPGA and PowerPC VXS multiprocessor designed to meet the signal-processing needs of modern signals intelligence, Software-Defined Radio, and radar applications. It features an onboard Xilinx Virtex-5 FPGA for the implementation of high-performance DSP applications. The FPGA processing is supplemented by a PowerPC for stand-alone operation, communications management, and user applications. Notably, the VXS-620 maximizes sensor I/O density with two PMC/XMC sites. These sites can support additional FPGAs, multiple channels of analog or digital I/O, and additional network interfaces. The VXS-620 is also supported by comprehensive Development Kits available for Linux and Wind River VxWorks. These include a Software Development Kit (SDK) with all necessary software drivers and libraries required to run the operating systems on the PowerPC. They also include an FPGA Development Kit (FDK).

www.nallatech.com **NALLATECH**

OpenVPX/ VPX-REDI/VPX SBC

General Dynamics' PX3030 is a 3U VPX-REDI/OpenVPX/VPX SBC. Conduction-cooled and military-rugged, it is designed for harsh-environment combat vehicle applications and supports 2-Level Maintenance applications. It features a Montevina platform Core 2 Duo CPU and the GS45/ICH9Me Express chipset. It offers scalable performance from low-power 1.2 GHz to high-performance 2.26 GHz processors, along with up to 8 GB DDR3 RAM. An extensive I/O complement – 2x GbE, 2x eSATA, 6x USB, 4x serial, 8x GPIO, RGB, and audio – is also provided, as is flexible expansion via a VITA 42.3 XMC site.

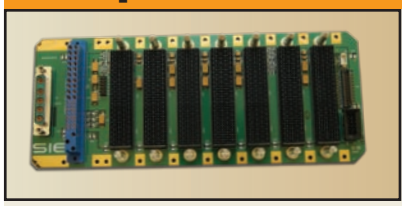
www.gdcanada.com
GENERAL DYNAMICS

3U VPX/OpenVPX RAID storage card

The 3U VPX cc SSD Raid is a rugged 3U VPX/OpenVPX conduction-cooled, high-speed SSD RAID storage card. It offers PCIe x8 lanes, along with burst write at 1.2 GBps and burst read at 1.3 GBps. Capacity is 4 TB or 8 TB, and power for 4 TB is <12.5 W typical, 17.5 W maximum. The RAID storage card withstands environmentals of 1,500 *g* shock, 16 *g* vibration, and -40 °C to +85 °C temp. MTBF is 1,500,000 hours, with 10-year data retention and 64-bit LBA support.

www.pcisystems.com
PCI-SYSTEMS INC.

3U VPX vetronics backplane



The I/O PLUS 3U VPX Full Mesh Backplane's "I/O PLUS" enables fit within a wide span of VPX applications and provides two front-edge, high-speed VPX connectors along with two interchangeable I/O daughtercards. The backplane is highly suited for the needs of aerospace and vetronics applications. Moreover, it utilizes more than 200 W for each VPX slot. J1 and J2 specifics include: J1 – 10 high-speed differential channels and fat pipes; and J2 – 20 single-ended signals and 16 fat pipes.

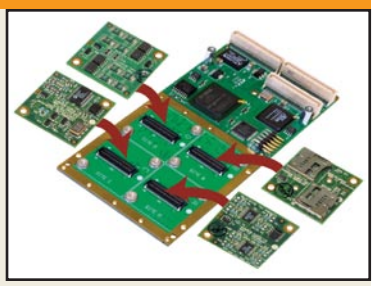
www.sie-cs.com
SIE COMPUTING SOLUTIONS, INC.

3/4 ATR forced-air chassis

Hybricon's 3/4 ATR Chassis takes customers from development to deployment with the same rugged 3/4 ATR 3U forced-air chassis. The chassis also offers support of 3U conduction-cooled payload for VPX/OpenVPX or CompactPCI bus architectures. Card cage choices include 6-slot 1.0" pitch or 10-slot 0.8" pitch plus 2-slot 0.8" pitch (power supplies). A Low Cost Development Version supports a standard backplane, cabled I/O, industrial-grade fans, and an external commercial-grade power supply; meanwhile, the Deployment Version supports a custom backplane, cableless I/O panel, MIL-grade fans, and 1 or 2 MIL-grade 200 W, 28 VDC-input power supplies.

www.hybricon.com
HYBRICON CORPORATION

Conduction-cooled PMC carrier



Technobox, Inc.'s 5918 is a conduction-cooled, PMC form factor carrier for the Technobox Micro Mezzanine System (MMS). The industrial temperature, RoHS-compliant FPGA-based carrier can accommodate up to four MMS Electrical Conversion Modules (ECMs) for assorted I/O interfaces. It is powered by an Altera EP3C16F484I7N with 16 K logic elements and easily configurable using Quartus and SoPC Builder. The carrier has 8 Kb memories, 18 x 18 multipliers, and PLL support, in addition to a 32-bit 66 MHz PCI interface at 3.3 V or a 5 V PCI interface (PLX PCI9056 PCI to 32-bit local bus).

www.technobox.com **TECHNOBOX, INC.**

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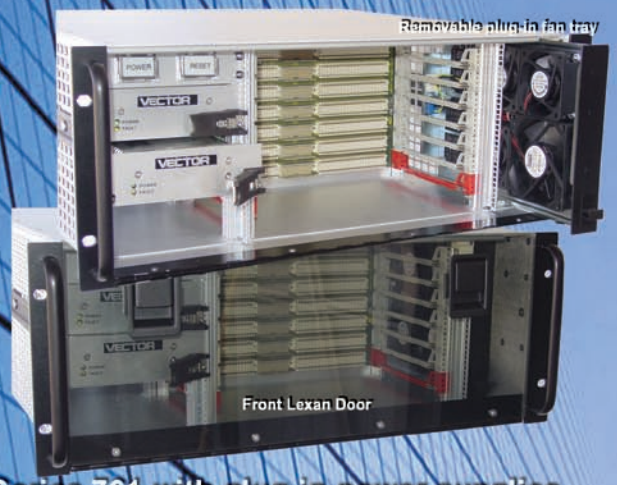

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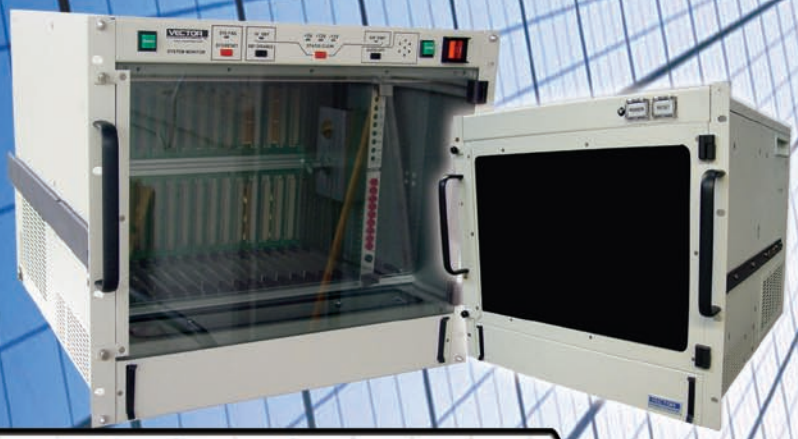

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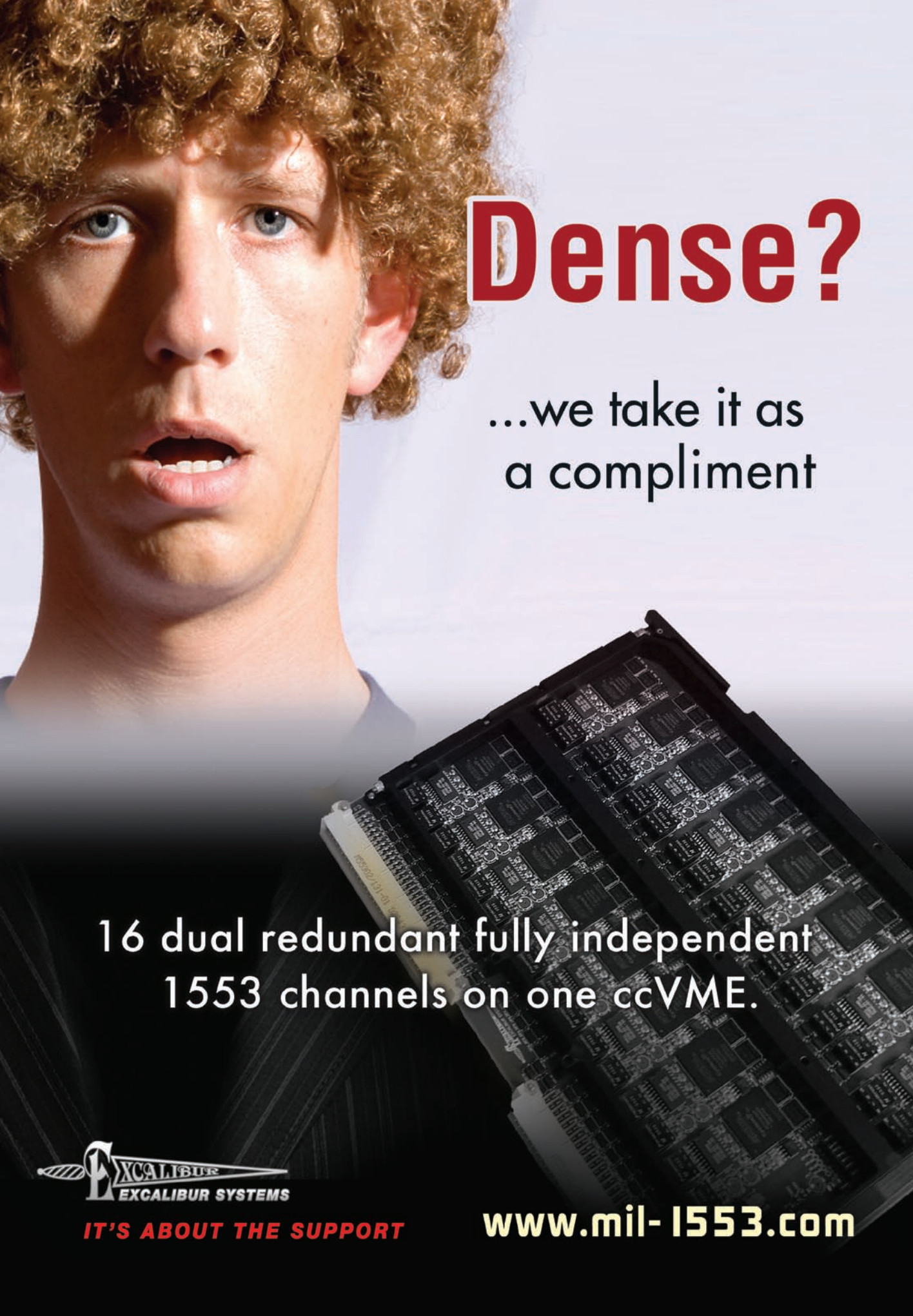
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VX3020

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