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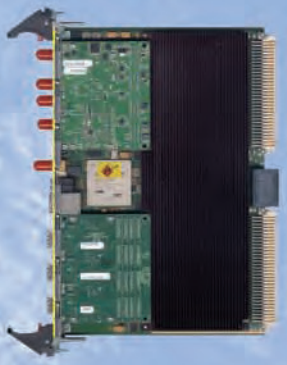

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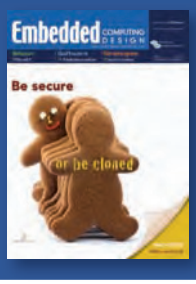
On the cover

If you spend your time trying to design something unique and different, it'd be a shame to have it copied. Yet many embedded designs suffer that fate due to a lack of hardware security practices. See our Strategies section starting on page 18 for ideas on how your design can remain uncloned.



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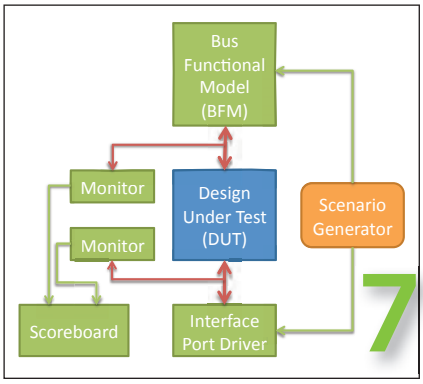

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What you're seeing throughout the magazine are 2D barcodes – our newest innovation for delivering information quickly and easily. The codes are in QR format, readable by a variety of barcode scanner software programs available on popular smartphones. Each barcode in this issue contains a URL, which you can access directly with your smartphone browser and e-mail or text to anyone.

QR code scanner software varies, so look for the one that works best for you. Here are some choices that can be found in your app store or online.

iPhone: App names like BeeTagg, ZXing, or QuickMark (staff favorite)

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BlackBerry: Try BeeTagg, UpCode, or ZXing

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Left to My Own Devices

Don Dingee

Don't bet against change

Betting against change in the technology world is a really, really bad idea.

Sure, sometimes technological change doesn't stick when it's too far on the edge or poorly implemented. But it's almost impossible to name a case where a newer solution got traction in an exciting way with the right audience and the previous solution survived.

In an interesting conversation I had at Embedded Systems Conference Silicon Valley (ESC SV) last month, a VP of marketing at a prominent firm told me that he saw industrial opportunities for embedded computing shrinking. That's probably true for traditional process control equipment, where inexpensive hardware continues to replace proprietary stuff. But once I told him I categorized smart energy as the new face of industrial, and he thought about it for a moment, he got it. Are you betting against smart energy? I seriously doubt it.

The same is obviously true for mobile and home embedded devices; growth in those markets has been and continues to be explosive, and it's not just among prosumers – it's reached the mainstream. Apple became a phone company? Yes, because they took their core competence of a user experience and made it stick. iPads are everywhere now as the change builds speed. Google became a phone company? User experience, again. Android is also building momentum fast.

The same thing is happening in automotive. The whole idea of bringing an individual's mobile device into a car and plugging that combination into the cloud for services is absolutely transforming the automotive industry. Go ahead, find your favorite stock charting site, type in the symbol "F," and what do you see – a stock that's doubled in a year. Coincidence? Granted, the cloud strategy isn't the only thing going in Ford's favor, but it is what is driving people into their showrooms. (Meanwhile, my 2007 Saturn Vue Hybrid is sitting at the dealer having its computer replaced for the third time in four years. Unexciting doesn't begin to describe my feelings there, and unfortunately the folks behind that product are paying with their jobs. Cloud computing? GM is still trying to spell it.)

The same thing is happening in medical. I breathed the word "Continua" just to get reactions at ESC SV, and it was amazing to see that people were not only very aware of the health alliance, but also were doing something with the idea of connected devices to help people be healthier. I had a super-exciting airport conversation with Jon Adams of Freescale Semiconductor heading home from the show, and I can tell you he's just starting to imagine the possibilities for how health monitoring improves lives and transforms health care.

The only world where the status quo pays is defense, and a really interesting transition is happening there – they are being forced to build their own processors in many cases, because no commercial vendor will keep theirs around for the life cycle defense customers think they want to see. Even that's a change not good to bet against.

Change for the sake of change isn't the idea. The folks that really listen to what the user wants, boldly go forward, and get it right can create a total shift. We're now entering a new cycle of that. Just look through this issue and see how FPGAs, mobile virtualization, and security devices are solving problems in ways we hadn't imagined a few short years ago. Then head to our website to see many more examples, or catch one of our E-casts.

Where have all the good times gone? In this industry, they're in front of us if we choose to look forward.

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Producing and verifying quality FPGA IP

By Jason Lawley and Jeremy Goolsby

There is more to verifying IP than functionality. Interaction of features, variability in timing, and testing strategies all factor into a broader verification strategy.

FPGAs have evolved in the past decade, becoming larger and more complex. The Intellectual Property (IP) developed for FPGAs has likewise increased in size and complexity. To deal with this increased complexity, IP developers have embraced best-in-class verification methodologies. Even when using these methodologies, developing IP for FPGAs still poses unique challenges that the typical ASIC designer might not encounter.

FPGA development presents three key challenges. One is that FPGA IP is often highly parameterized, which can create a very large number of design variations to test. Another issue is that FPGA IP developers need to verify that timing can be met once integrated into the user design. Finally, the IP developed for FPGAs is more susceptible to architectural changes than IP developed for other platforms. It is important that the verification environment accommodates these architectural changes as quickly as possible with a minimal amount of work.

Parameterize features

An FPGA has a higher cost per gate than a corresponding ASIC, so designers targeting an FPGA are motivated to create IP that does not consume any more resources than what is necessary. Whereas the ASIC will implement all supported features, the FPGA has the option of implementing only the features that the customer needs. Therefore, FPGA IP can and should be parameterized so that synthesis will remove unwanted logic. As an example, the size of the Xilinx 10 GbE MAC core shrinks by about 25 percent if the Ethernet Statistics Gathering feature is not needed, freeing up FPGA resources for other logic.

When scoping out what will be parameterized, factors like data bus width, number of pipeline stages, and optional functionality are good candidates to consider because they permit the designer or customer to make trade-offs between performance and resources consumed. Further trade-offs can be made by parameterizing platform-specific features like Block RAM and DSP blocks, as opposed to using fabric logic.

The downside is that every added parameter creates another permutation that must be tested. How does the verification engineer know the parameter has been exercised for all values? The best way to do that is through gathering coverage statistics and analyzing the coverage reports produced by the simulator. For instance, if a design has a Data Width (DW) parameter that controls whether the IP uses a 32-bit or a 64-bit data path and a Pipeline (PL) parameter that controls whether it uses extra pipelining to help meet timing, a basic coverage report with simple cover points might show that both values of DW and PL were exercised. However, it would not show if a 64-bit data path was tested with no extra pipelining. To achieve that, SystemVerilog "crosses" and/or more complex cover points are used to report if a particular combination of parameters has been hit.

For a large set of parameters, it quickly becomes apparent that hitting every permutation will take forever if every parameter is allowed to be randomly set. The verification engineer has to define the subset of parameter permutations that are relevant and heavily weight those that are more likely to be used by end customers. Additionally, permutations that better exercise the design should be chosen, such as those that induce full FIFO conditions or rarely used state transitions. Constrained random verification is ideal for this purpose because it allows the tool to randomize parameter values according to the verifier's constraints and uses coverage metrics to see if important permutations are being hit. If they are not, then the verifier can either run more tests or change the weighting of the constraint's distribution of values.

Verify timing

One of the challenges FPGA IP developers face is ensuring that the IP can meet timing once integrated into the customer design. Because it is difficult to functionally verify designs with a large parameter space, it is similarly difficult to understand the effects of the parameters on the ability to meet timing. Another hurdle for the developer is that the IP might compete for FPGA fabric resources with other portions of the user's design, which can make it more difficult to meet timing.

Developers can employ multiple techniques to help ensure the IP will continue to meet timing even when integrated into the user's design. A representative example design is nice to have, but not necessary. If an example design is not available, double-register all I/O that will go to the FPGA fabric. I/O that go on or off of the chip should be connected to the appropriate locations.

Once the design is in place, the next step is to implement the design in the targeted FPGA architecture. As part of the testing process, overconstrain the IP clock frequencies by 15 percent. Also, add an area constraint to the IP so that it is constrained to a region of the FPGA fabric that is not much larger than its minimal needs for placement, as shown in Figure 1. This will emulate congestion for when the IP is integrated into the user design.

The final step is to ensure that different parameter settings do not have an adverse effect on the ability to meet timing. Identify key parameters that are most likely to have an impact on timing closure. Randomize the identified parameters, run with the area constraint and higher clock frequencies, and ensure timing can still be met in all of the FPGA devices that the IP targets. The more combinations of parameters that developers run, the greater their confidence will be that the IP will meet timing in even the most difficult customer environments.

The more combinations of parameters that developers run, the greater their confidence will be that the IP will meet timing in even the most difficult customer environments.

Decouple test scenarios from implementation

A designer might need to change the latency or data path width of the core late in the design cycle, either as a response to place and route indicating that the design will have difficulty meeting timing, or to take advantage of an FPGA that is faster and/or has a different number of resources. If the verification engineer did not anticipate that kind of change (for example, the test scenario assumed a fixed latency), then a large number of tests might need to be changed to code the new expectation. A well-designed verification environment will need few if any changes to respond to this.

One of the best methods to decouple the test bench environment from the Device Under Test (DUT) implementation specifics is to use a scoreboard, as depicted in Figure 2. The test scenario pushes the expected results (for instance, packets) into the scoreboard, and as the DUT produces the data, it is compared to the scoreboard version automatically by the test bench. The test scenario does not need to be concerned when the DUT produces the data, only what data it produced.

Additionally, if the width of the data path changed and the data produced by the DUT is divided over several additional cycles (or unified into fewer cycles), then the scoreboard provides a

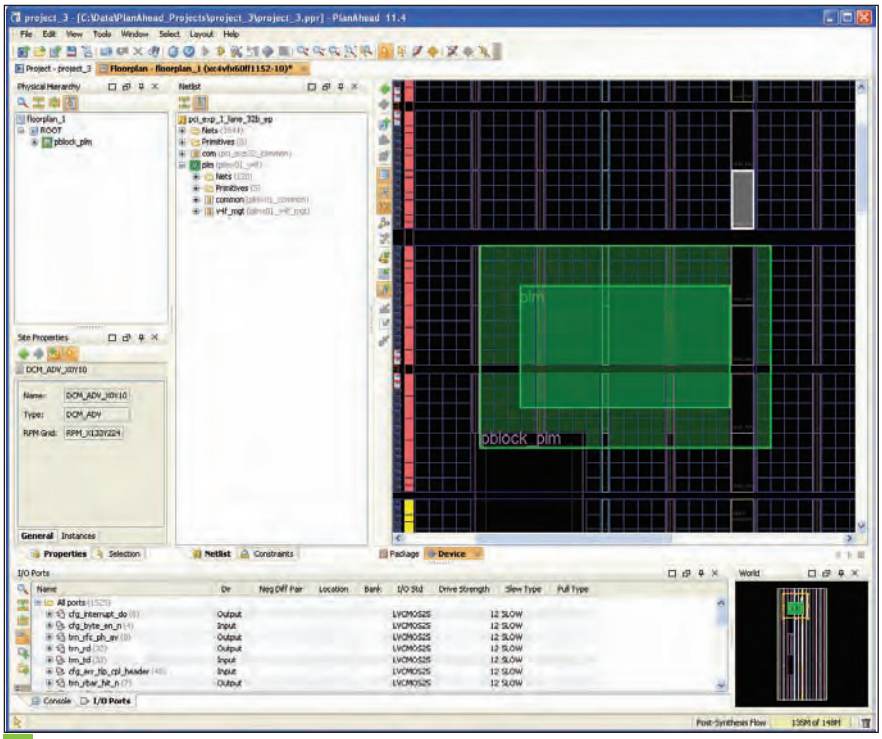

Figure 1 | An IP block in the Xilinx PlanAhead tool is constrained to a small region of the chip to emulate congestion for when the IP is integrated into the design.

single point in the test bench wherein the comparison to that expectation can be changed. The alternative option to hard-coding the expectation in the test scenario requires that each scenario be updated when the DUT's data width or data format changes.

Port drivers and monitors need to be coded to anticipate interface changes. An up-front effort that allows these modules to connect to ports and interfaces of different data widths can pay off later in the design and verification cycle when quick adaptations are needed.

FPGA IP, verified

The amount of IP available for FPGAs has increased tremendously during the past several years. To be competitive, vendors must consistently meet expectations for quality. Because time-to-market needs for FPGA IP are becoming more aggressive, vendors must do everything possible to prevent a delivered core from having issues that can slow down its customers. This means that well-thought-out verification strategies that can adapt quickly are a must. ECD

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Jeremy Goolsby *is a staff engineer in the IP Solutions Division at Xilinx. He has 12 years of experience designing FPGA IP and holds a BSEE from the University of Illinois and an ME from the University of Colorado.*

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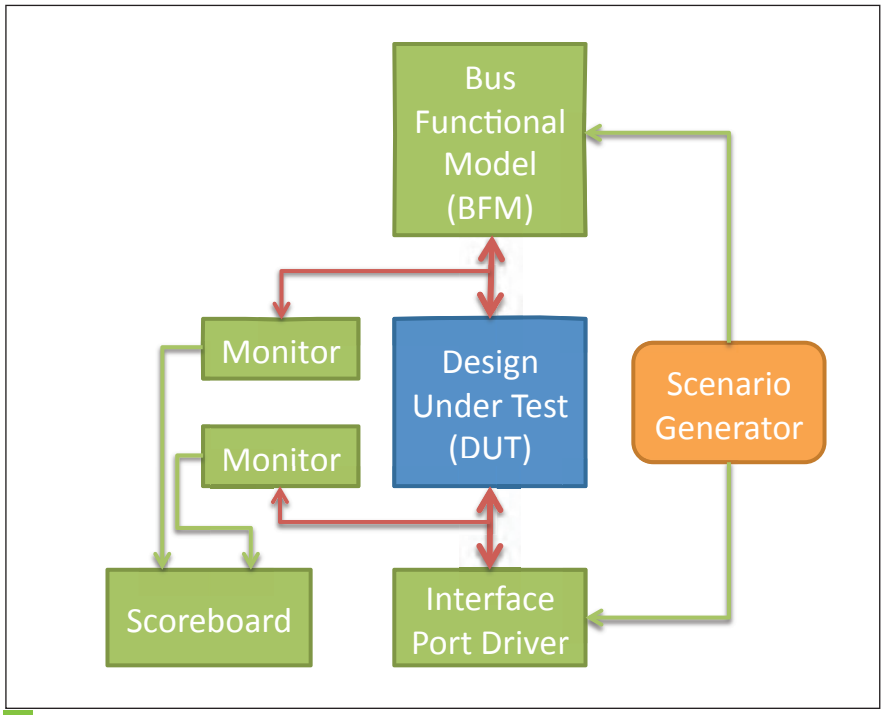

Figure 2 | Using a scoreboard is one of the best methods for decoupling the test bench environment from the device under test.

Implementing PCI Express bridging solutions in an FPGA

By Sidhartha Mohanty

One advantage of using FPGAs is the ability to implement proven intellectual property to complete bridging functions quickly and with confidence. A look at a common but complex interface, PCI Express, demonstrates these benefits.

Like its predecessor, the Peripheral Component Interconnect (PCI), PCI Express (PCIe) is becoming a ubiquitous system interface. Unlike PCI, PCIe adopts a SERDES interface to provide users with the scalability required for future applications. As system bandwidths increase, more applications are moving to SERDES-based interfaces like PCIe. In the past, Application-Specific ICs (ASICs) and Application-Specific Standard Products (ASSPs) were typically used to implement next-generation interface solutions. ASICs and ASSPs were popular choices because they provided a low-cost, low-power design solution.

However, several new FPGA families present attractive options for PCIe interfaces. FPGAs provide an adaptable platform without the inflexibility of ASSPs or the long lead times and large nonrecurring engineering costs typically associated with ASICs. Newer-generation FPGAs with embedded SERDES offer designers an extremely rich, high-value programmable architecture in a low-cost, low-power solution for serial interfaces. The same FPGAs can be used to support a variety of serial protocols like PCIe, GbE, SGMII, XAUI, Serial RapidIO, and others, providing a single FPGA platform for multiple designs.

PCIe is also becoming the interface of choice for control plane applications, replacing older parallel interfaces like PCI. Newer-generation devices use one or more PCIe links. In most devices, the PCIe core is implemented as a PCIe endpoint. Designers often need to connect these devices to previous-generation devices that have a parallel bus (such as microprocessors with parallel bus interfaces). Using a low-cost, low-power FPGA to bridge between PCIe and a parallel interface provides designers the flexibility to solve this problem without exceeding their system cost and power budgets.

Design challenges

As designers migrate from PCI to PCIe, the intricacies of the protocol coupled with the complexities involved with SERDES-based designs pose significant challenges. Fortunately, FPGAs combined with a full-featured PCIe IP core, reference designs, hardware evaluation boards, and associated demos help smooth out the otherwise steep learning curve PCIe designers face. FPGAs are an ideal platform for PCIe-based applications. Because they are programmable, FPGAs give designers the flexibility to resolve design issues late in the design cycle with rapid turnaround times. Designers can readily change or add features as individual design requirements evolve.

FPGA designs also allow designers to make updates to accommodate changes to the specifications, enabling them to future-proof their designs against obsolescence. The programmable platform enables designers to use the same FPGA to implement interface solutions that connect to a broad variety of other PCIe chipsets: endpoints, root complex, or switches. The designer can integrate other functions required by the system in the FPGA, reducing the number of components on the board and further decreasing the total cost of the system.

Bridging interfaces

FPGAs provide an extremely flexible, programmable platform for system designs. A comprehensive solution package that includes IP cores, hardware platforms, demo designs, drivers, and software enables designers to shrink their development cycles while reducing the complexity of the design.

One common design requirement is for a PCIe solution to bridge between PCIe serial interfaces (endpoint devices) and legacy parallel bus interfaces, as shown in Figure 1. An FPGA with a PCIe root complex IP core provides designers

with the basic building blocks needed to implement such a solution. Alternatively, ASSPs and ASICs can also implement this function. However, unlike FPGAs, these devices can implement only a fixed configuration that cannot be changed to accommodate the various parallel bus interfaces available.

A programmable FPGA platform, on the other hand, enables designers to make specific changes in their design to implement the specific bridge function that matches the interface available on their particular board. Designers also have the flexibility of implementing multiple bridges or different configurations of bridges in a single FPGA, thus reducing the total components on the board. An FPGA coupled with the PCIe root complex IP core can enable several other bridging solutions as required by a design.

PCIe root complex

A PCIe endpoint operates as an upstream device, a function that a root complex device can perform. However, a full-featured root complex implementation is quite expensive in terms of FPGA gates used. Instead, a lightweight root complex core with a subset of the transaction layer functionality is adequate for implementing most bridging functions.

As shown in Figure 1, the bridge comprises two basic building blocks. The first block is the PCIe root complex (or Root Complex-lite) IP core, which interfaces with the PCIe endpoint device. The second block is the bridge logic that interfaces to the local bus/parallel interface. Because this implementation is in a programmable FPGA, the designer has flexibility to customize the design based on specific interface needs. Other functionality can also be integrated into the same FPGA, eliminating other components on the board and reducing overall bill-of-materials costs.

Implementing lighter IP

PCIe is a complex protocol. Providing fully functional, fully validated PCIe IP cores significantly reduces design complexity. For example, Lattice Semiconductor's PCIe Root Complex Lite (RC-lite) core implements a x1 or x4 root complex function primarily for use

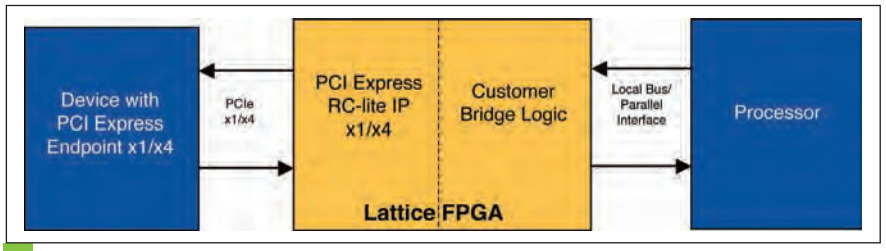

Figure 1 | An FPGA with a PCIe root complex IP core bridges between PCIe serial interfaces and legacy parallel bus interfaces.

in PCIe bridging applications. As shown in Figure 2, all of the PCIe layers are implemented as a combination of embedded ASIC blocks and the PCIe RC-lite soft IP core implemented in the FPGA. The various blocks include the electrical SERDES interface, physical layer, data link layer, and a minimum transaction layer to support the protocol stacks required to implement a PCIe root complex function. This lighter IP is optimized for use in simple bridging applications between a PCIe endpoint interface and a parallel local bus interface.

The PCIe RC-lite IP implemented in a LatticeECP2M or LatticeECP3 FPGA enables low-cost, low-power PCIe bridging applications while providing designers the flexibility to customize the bridge interface. Additionally, PCIe hardware evaluation boards and a variety of reference designs, demos, and software drivers help designers kick-start their PCIe designs and reduce time to market. Lattice also provides a hardware evaluation board for designers to test the RC-lite IP solution. Designers can complete interoperability and verify the system-level functionality of these solutions prior to deployment, saving the time and cost normally associated with post-design debug and performance enhancements.

Bridging complexity simplified

PCIe designs pose significant challenges to designers. The requirements for the interface are varied, depending on whether the PCIe device has to connect to another endpoint, root complex, or switch. Furthermore, designs often require a connection between a PCIe endpoint device and another device with a parallel bus interface.

Designers can implement these functions in a low-cost, low-power FPGA platform while retaining all the benefits of a flexible programmable architecture. Using a PCIe root complex IP function in an FPGA provides an ideal platform to implement these bridging functions. ECD

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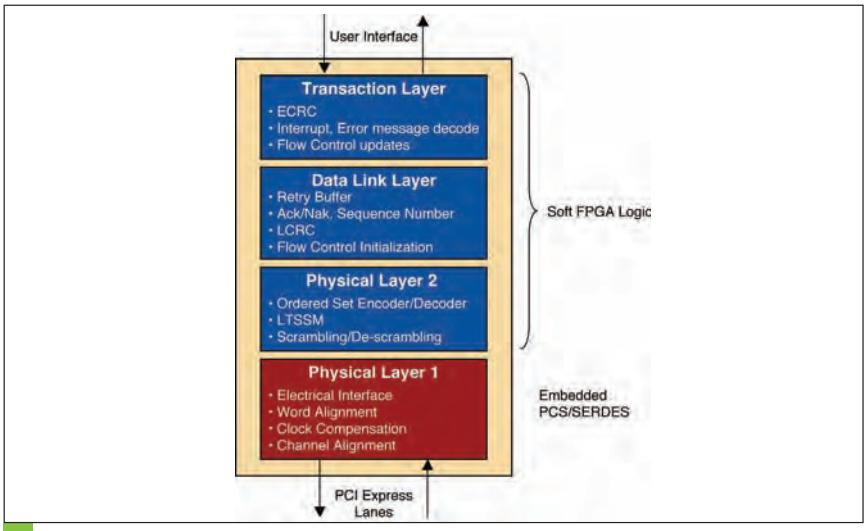
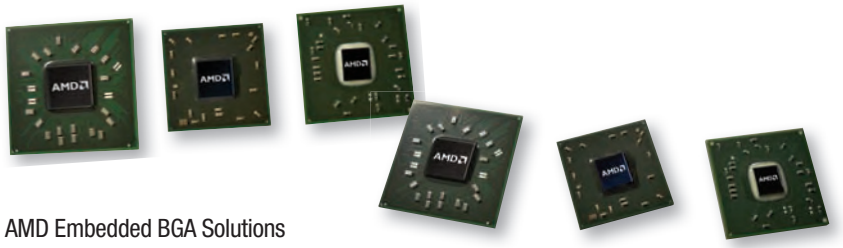


Figure 2 | The PCIe RC-lite IP protocol stack helps reduce design complexity in PCIe bridging applications.

Making high-performance, power-sensitive, dual-core applications affordable

By Cameron Swen



AMD Embedded BGA Solutions

What are your choices when your application's performance requirements, power limits, and budget conflict? Comparing the options available today reveals some important differences that can affect the bottom line.

AMD made a lot of noise recently with the announcement of a new embedded Ball Grid Array (BGA) platform that was rolled out at this year's Embedded Systems Conference in San Jose. This new BGA-packaged solution for the ASB2 socket touts better performance per watt than the previous generation, with a new 128-bit floating-point unit, wider instruction fetch, reduced latencies, and large page support.

AMD is providing ample versatility through the option of a 1 GHz single-core CPU with a Thermal Design Power (TDP) of just 8 W. For multithreaded applications, you could drop an 800 MHz dual-core CPU in the exact same thermal envelope. There are additional high-performance dual-core CPU options at 12, 15, and 25 W TDP. The power of the companion AMD 785E chipset can be scaled between 6.4 W and 13 W depending on the system's needs, making it a strong choice for applications such as portable instrumentation, industrial controls, and automation. For applications that are I/O-intensive or require real-time performance, this new platform operates at less than 20 W TDP and offers the high throughput and low latency of AMD's Direct Connect Architecture.

But this platform isn't just about the processing capabilities. When you consider the AMD 785E chipset's integrated ATI Radeon™ HD 4200 graphics, it's clear that AMD is offering a top-to-bottom solution that aims at graphics-intensive applications such as digital signage, where manufacturers want to integrate the processing solution into the back of the display and need high-quality and high-performance graphics. For a high-performance application such as this, a 2.2 GHz processor can be paired with the AMD 785E chipset, and the entire solution can still operate within a 40 W envelope. For an extra boost in graphics performance, the 785E also supports enhanced operating modes that allow it to boost the graphics core up to 590 MHz.

The versatility of this platform doesn't stop there. For applications that demand reliability such as Small Office, Home Office (SOHO) servers and storage applications, it also supports Error Correction Code (ECC) memory, making it a good option for applications like integrated medical appliances, point-of-sale systems, and kiosks that need to operate reliably over long periods of time.

This sounds good, but how does this platform stack up against competitors' solutions? Pretty darn well. The entire AMD solution's power envelope is comparable to Intel's BGA-packaged Core i7 solutions for embedded, both ranging roughly between 20 W and 40 W with the chipset. Although the Core i7 with the QM57 PCH is a two-chip solution, the footprint on the board is a mere 4 percent smaller than the ASB2/785E chipset, at 1,627 mm^2 and 1,699 mm^2, respectively. And when it comes to board layout, the Intel solution has 414 more balls for you to route, with 2,359 versus 1,945 on the AMD solution. The real difference is the price. Based on the March 28, 2010 Intel Processor Price List, the 1K tray unit price for the LV/ULV Intel Core i7 processors ranged from $278 to $332 for just the processor. In contrast, the small quantity price for the dual-core versions of the second-generation AMD BGA platform solution (including the chipset) is set to roll out between $127 and $196.

So whether you are designing a graphics-intensive integrated digital signage system, an I/O-intensive real-time industrial controller, or a high-reliability SOHO server, the new AMD embedded BGA platform solution will likely be the best choice for overall performance, power efficiency, and bottom-line value.

Cameron Swen *is a senior manager of product marketing in AMD's Embedded Solutions Division. He works with customers and partners to deĀne products and strategies for various embedded markets. Cameron joined AMD in 2003 as manager of technical marketing for AMD's Innovative Solutions Group. He started his career 17 years ago as an engineer working with embedded computer systems and has held technical marketing positions at National Semiconductor and AMD for the past 10 years. Cameron holds a degree in Engineering from Colorado State University.*

AMD
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Getting the most from multicore silicon with embedded virtualization

By Rob McCammon

Virtualization in embedded applications has much in common with its enterprise and desktop equivalents. Unique embedded use cases and specialized underlying technology offer developers new opportunities to optimize designs for performance and responsiveness.

Adoption of multicore technology on the desktop, in the data center, and now in embedded designs responds to comparable needs – scaling compute capacity without stepping up system clocks and attaining more MIPS per watt for next-generation devices and applications.

Mainstream multicore on the desktop and in data centers requires Symmetric Multi-Processing (SMP) support from deployed Operating Systems (OSs). The Linux kernel has supported SMP for almost a decade, and SMP-capable Windows and Mac OS versions are widely used today.

By contrast, embedded OSs are trying to catch up to support multicore CPUs. Even as OSs become more adept at running in multicore environments, applications and middleware still face the challenges of thread safety, concurrency, and load balancing.

Virtualization software architectures

To solve these challenges, different virtualization strategies have emerged, starting with Type I and Type II, as shown in Figure 1. In Type I virtualization, the hypervisor "owns" the CPU and is responsible for booting and running guest OSs. Type I platforms are "lean, mean," and mature, emerging from generations of development for mainframes and minis, and now for mobile devices. By contrast, Type II virtualization offered by platforms such as VMware Fusion, Parallels, and Sun VirtualBox focuses on end-user experience, with the hypervisor running as an application over another OS with no performance guarantees.

Embedded virtualization follows its own paradigms. In infrastructure applications like routers, switches, and gateways, use cases resemble the enterprise. Type I hypervisors host instances of Linux or a Real-Time OS (RTOS) to support virtual appliances (firewalls, deep-packet inspectors, and other appliances) on a single piece of hardware or virtual spares in a redundant high-availability architecture.

In mobile devices, OEMs use bare-metal virtualization to consolidate multiple CPUs to run baseband, multimedia, and application stacks and diverse OSs (Android or Linux in one or more virtual machines, and an RTOS in another) on a single CPU to save bill-of-materials costs.

Going for multicore

In addition to hardware consolidation, virtualization provides a good mechanism for

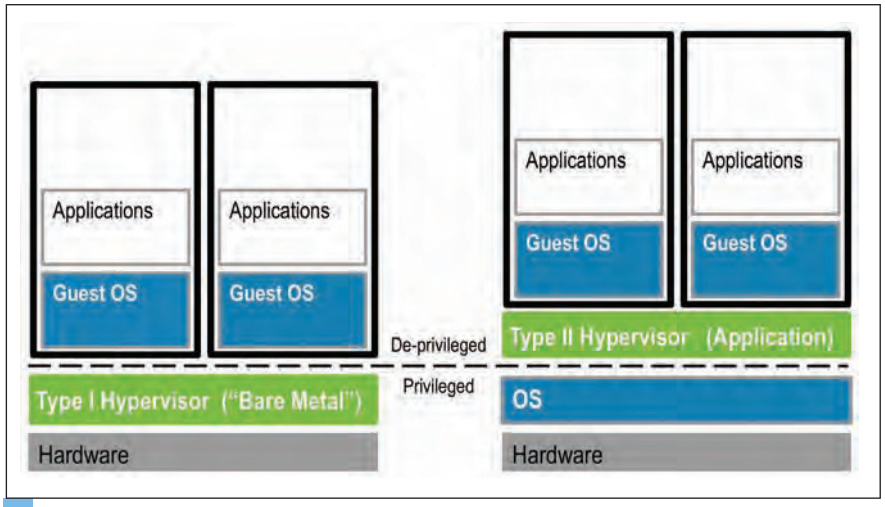

Figure 1 | Whereas a Type I hypervisor boots and runs guest OSs, a Type II hypervisor runs as an application over another OS.

distributing existing loads across multiple cores in a single processor. Embedded OS architects tend to see multicore silicon as a collection of discrete CPUs. Most legacy RTOS multicore support reflects this perspective, with requirements for unique copies of the OS and stacks running quasi-cooperatively on separate cores.

As RTOS suppliers begin to create multicore versions of their wares, they often use static mapping of loads to cores in multicore silicon. Some embedded virtualization platforms require static assignment of hypervisors and the loads they host and run (that is, one hypervisor per CPU core, as shown in Figure 2).

Static mapping of physical silicon to virtualized loads is inefficient and fails to deliver the advantages conferred by virtualization. A more effective approach is provisioning each guest OS with a virtual CPU that can map to a single CPU (one-to-one), share a CPU (many-to-one), or spread across multiple cores (one-to-many), as depicted in Figure 3.

Mapping loads to virtual CPUs to physical cores can be locked at integration or varied to balance loads, as demonstrated in the following applications.

Load balancing

Today's networked devices – mobile phones, set-top boxes, in-vehicle systems, network appliances, and almost any type of intelligent device – are application platforms with loads as varied and complex as desktop computers, data center blades, and servers. Multicore CPUs promise high throughput and zippy response from

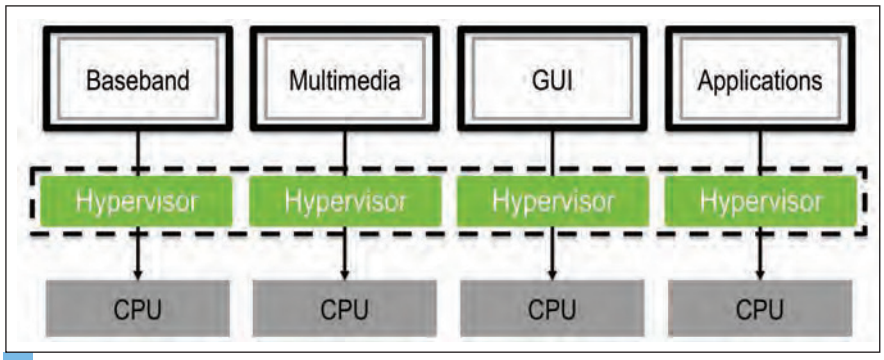

Figure 2 | In static mapping of loads, one hypervisor is assigned per CPU core.

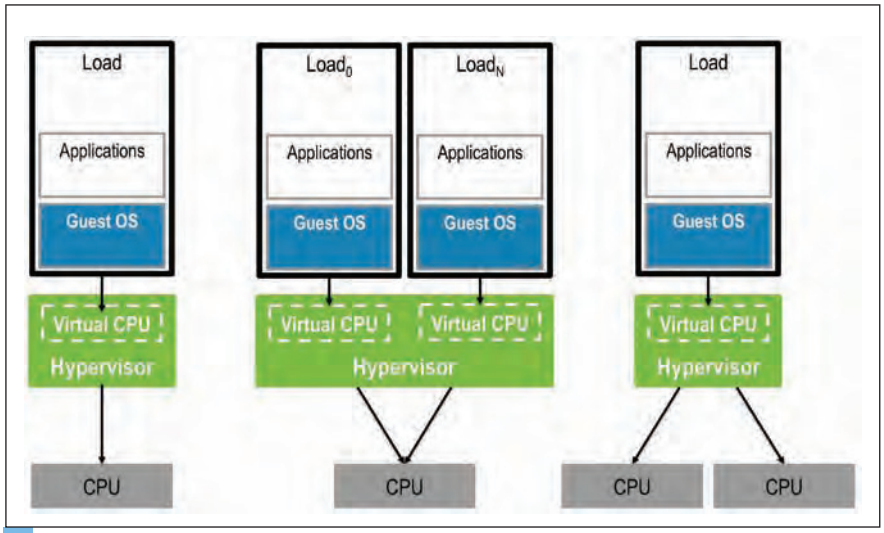

Figure 3 | Virtualization enables one-to-one, many-to-one, and one-to-many mapping of loads to cores.

modern embedded software, but loading and core utilization prediction outstrips the process of integrating software from varied sources, especially from app stores.

Virtualization gives developers and integrators additional tools for optimizing device performance. An embedded hypervisor can monitor the loads of guest OSs and host policy software to allocate CPU cycles and other resources accordingly.

Multicore power management

Multicore systems can present steep challenges to power-management schemes optimized for single-core systems. In particular, many multicore Systems-on-Chip (SoCs) limit the scope and capability of Dynamic Voltage and Frequency Scaling (DVFS):

- SoC subsystems and multicore CPUs usually share supply voltages, clocks, cache, and other resources, meaning DVFS applies to all cores.
- Scaling voltage on one SoC subsystem (when possible) can limit communication with other subsystems over local buses and deny access to shared memory, including the subsystem's own DRAM.
- Clock scaling of single SoC subsystems limits interoperability, especially for synchronous buses.
- Some operations use cores at full throttle or not at all, but others impose varying loads. All-or-nothing use is easy to manage, but dynamic loads on multiple cores present much greater power-management challenges.

Now add multiple OSs. High-level OSs typically include DVFS power management such as Linux Advanced Power Management and Dynamic Power Management as well as Windows/BIOS Advanced Configuration and Power Interface. Most RTOSs avoid operations that limit real-time responsiveness, and when they do offer explicit power-management APIs like vxLib's vxPowerDown(), they do not have power-management policies. Even if one OS is capable of managing power in its own domain, it will have no awareness of the capabilities and state of its peers in the same system.

DVFS delivers energy efficiency by reducing voltage and clock frequency. DVFS-enabled CPUs offer safe operating points at fixed voltages and frequencies. As load/demand increases or decreases, power-management middleware or OSs transition from operating point to operating point, as illustrated in Figure 4.

A logical extension of DVFS is reducing voltage to 0 VDC and stopping the CPU clock by utilizing only two operating points – full stop and full throttle – applied across the range of available cores. This neat trick is only possible with virtual CPUs (refer to Figures 3 and 4) for mapping loads to physical silicon and migrating running loads transparently across CPU cores. Shutting down whole

cores is easier to manage than DVFS and leads to linear, predictable performance-energy trade-offs.

Multicore baseband

With the advent of high-bandwidth 4G networks, particularly LTE, mobile devices need to dedicate more processing power to wireless data communications. To enhance throughput with higher concurrency, emerging requirements call for dedicating entire cores to 4G I/O operations. This requirement has wireless chipset vendors and legacy RTOS suppliers scrambling to retool baseband OSs and software stacks for SMP operation.

The easier solution is to use mobile/embedded virtualization to enhance 4G throughput. Instead of dedicating two, four, or more cores to baseband processing, a hypervisor can map available cores to input or output operations as needed and scale back that mapping to support other CPU-intensive operations or perform per-core power management.

Only virtualization scales

Multicore software design is both more complex and simpler than meets the eye. Designers should resist the temptation to assign legacy software elements wholesale to available cores on next-generation embedded silicon.

Processor roadmaps point to further multiplication of available processor cores: today 2x on embedded CPUs, and soon 4x, 8x, and beyond. This surfeit of silicon will quickly outstrip static methods for provisioning and managing multicore software loads.

Only embedded/mobile virtualization can provide a scalable and flexible mechanism for realizing the benefits of multicore processing power and simplify system design, integration, and deployment, while making those systems more reliable and secure. **ECD**

Rob McCammon *is VP of product management for Open Kernel Labs (OK Labs). His prior experience includes marketing positions at Wind River, Integrated Systems, Software Development Systems, and Mentor Graphics/Microtec Research as well as engineering and technical sales roles at Hughes Electronics and HP. He holds a BS in Computer Engineering from the University of Illinois at Urbana-Champaign, an MS in Computer Engineering from the University of Southern California, and a Master's of Management degree from Northwestern University.*

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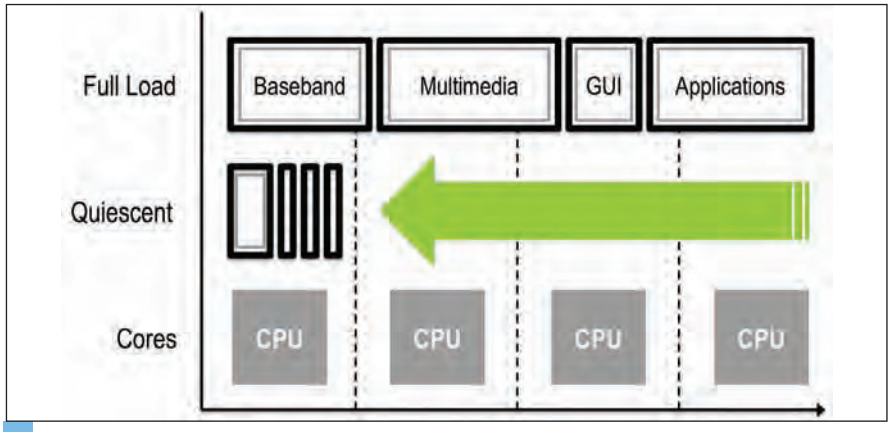

Figure 4 | With Dynamic Voltage and Frequency Scaling, loads can be migrated across cores to save power.

Hardware authentication secures design IP and end-user experience

By Robert Rozario

Photo source: www.flickr.com/photos/anonymouscollective/2291896028

Ensuring that a device is authentic without using an overly complex and expensive scheme to do so is one of today's many embedded design challenges. A chip-based implementation of elliptic curve cryptography can provide a secure solution at the right price.

Protecting electronic systems from counterfeiting is a growing challenge for OEMs. With the move to outsourced manufacturing for consumer electronics and computer peripherals, it is increasingly difficult to protect IP and prevent unauthorized production of devices using an OEM brand.

The problem is bigger than it might appear at first glance. For companies that offer a core system at subsidized prices, expecting to earn profits in aftermarket sale of accessories or consumables, counterfeit devices threaten both the business model and brand reputation. Some companies have even reported incidents of non-OEM accessories such as battery packs reaching end users and creating a potential liability.

Hardware authentication: challenges and selection criteria

Many classes of aftermarket parts and accessories such as notebook AC adapters and batteries are built to be compatible with OEM specifications and standards. In the midst of legitimate accessories manufactured by authorized third parties, there are counterfeit devices that are exact or near-exact replicas of authorized products.

The challenge is enabling a system to distinguish between authorized and unauthorized parts or between the OEM brand and third-party brands. While there are many tactics to address counterfeiting threats, each has its limits. Patents, custom connectors, and proprietary hardware/software solutions are used with varying success rates.

A relatively new approach is the concept of embedded authentication hardware, which can be used to ensure that an accessory or peripheral is authentic for use with a given system. In this type of solution, the authentication hardware is located in the accessory and the software resides in the host system.

A software-to-hardware authentication solution should address the following questions to protect against counterfeiting:

1. Is the host system immune to attacks?
2. Is the peripheral or accessory immune to attacks?
3. Is it possible to break one device and use the information to hack all the systems?
4. Can the security infrastructure extend to protect legitimate aftermarket parts?
5. How can one warn about the reuse of expired or unwarranted parts/accessories?
6. Is the solution cost effective and easy to implement?

In response to the final question, embedded security using a software to hardware authentication solution can meet both cost and ease-of-implementation targets for price-sensitive consumer electronics while still addressing the other questions.

Chip-based product authentication

Infineon Technologies provides chip-based security solutions for many applications, including e passport, Trusted Platform Module (TPM), and payment and chip card devices. The company recently added the Origa Original Product Authentication Solution (SLE95050FX) to its portfolio, drawing on two decades of security chip experience to address counterfeit protection in cost-limited applications.

The chip supports asymmetric authentication using discrete Elliptic Curve Cryptography (ECC) logarithm implementation, a mathematically complex and highly secure form of ECC. It stores data such as the private key, unique chip ID, and other customer information in a protected memory space secured from modification. Up to 192 bits of read-only data can be written into this space.

Additionally, the chip offers unprotected and freely usable nonvolatile memory of 512 or 704 bits for different purposes such as traceability of the manufacturing and

logistics chain, OEM-added data about the accessory, or documentation of end-user behavior such as the charging cycle. One version features an integrated temperature monitoring sensor to simplify the implementation of rechargeable batteries.

As depicted in Figure 1, an authentication solution consists of a host device serving as the master communicating through a Single Wire Interface (SWI) to the accessory containing the SLE95050. The chip can be directly or indirectly powered via the SWI interface, as shown in this illustration.

Symmetric versus asymmetric cryptography

An important consideration in counterfeit protection is the cryptographic system used. In consumer electronics and computers, the shared secret scheme or symmetric solution (in which the host and peripheral share the same secret) falls short. If the host shared secret is exposed, then original devices can be easily replicated into counterfeits guaranteed to work with all host systems.

Asymmetric cryptography uses two different keys for encryption and decryption.

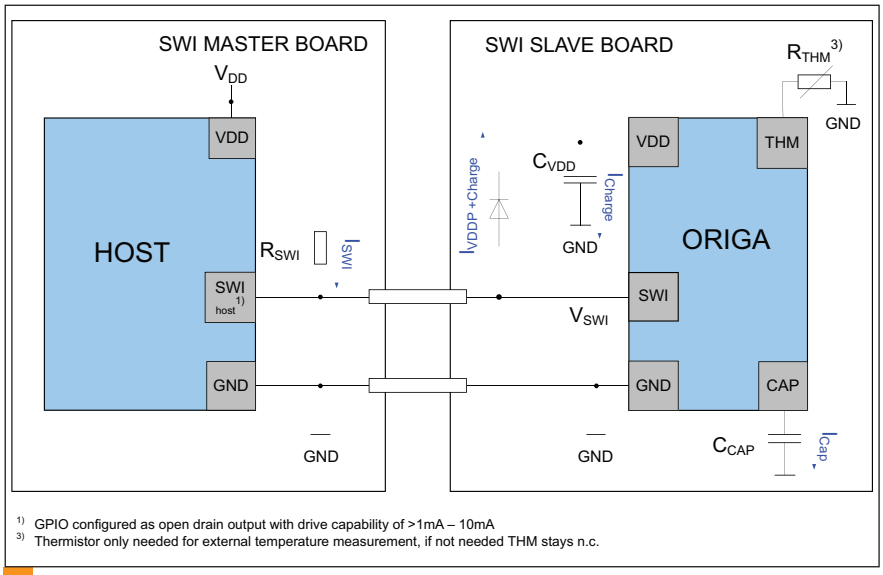

Figure 1 | In an anti-counterfeit system, chip-based authentication can be powered via a Single Wire Interface (SWI).

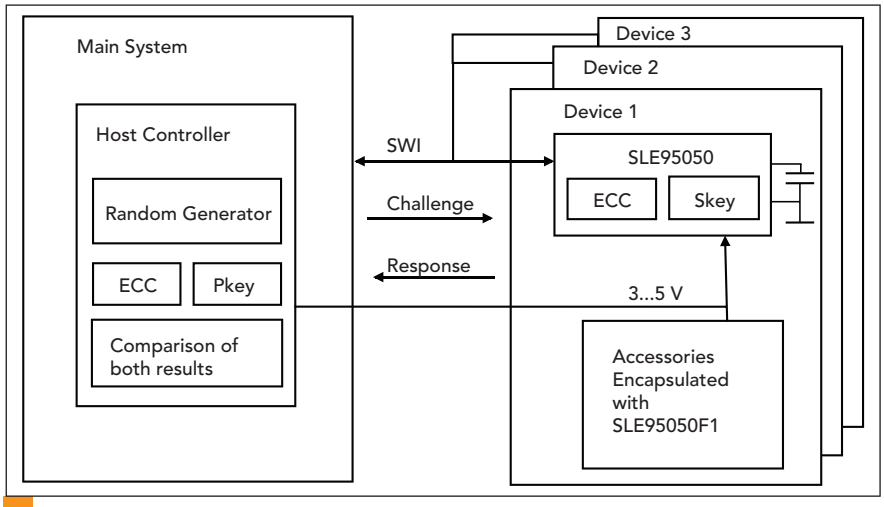

Figure 2 | A software-to-hardware authentication implementation allows the public key to be made public provided that the private key is kept safe in a chip embedded in the peripheral.

The so-called public key can be made public (and therefore used in the software that resides in the host system), as long as the other secret or private key is still in the safe environment of a chip embedded in the peripheral. This concept is illustrated in Figure 2.

Now let's take a look at how the software-to-hardware system addresses the challenges involved in implementing a robust authentication solution.

1. Is the host system immune to attacks?

Attacks on host systems are aimed at retrieving the secret that would allow successful counterfeiting. In software-to-hardware authentication, host code and libraries only contain public information. An attack on the host is therefore futile. From this perspective, the system is immune to attacks.

2. Is the peripheral or accessory immune to attacks?

The authentication chip incorporates physical security to protect its secret. Due to the ECC asymmetric protocol, bus snooping will not reveal any secrets. The chip implementation also includes protection against replay, side channel, and power attacks. Hence, the solution is relatively immune to attacks.

3. Is it possible to break one device and use the information to hack all the systems?

Since the host only contains public parameters and the chip contains the secret key and parameters, it is not possible to extract private information by manipulating the host. Also, hardware personalization at Infineon's Common Criteria EAL5+ certified facility prevents secret leakage from accessory manufacturing sites.

4. Can the security infrastructure extend to protect legitimate aftermarket parts?

The security system offers a personalization step that takes place in a secure Infineon facility. Personalization is possible for each particular customer or for each stock-keeping unit or subgroup of products for the same customer.

Personalized devices are supplied only to customer designated manufacturing sites and are not available for purchase by any other entities. The secure personalization process serves several purposes:

- Protects from a purchase of blank chips in the open market that are then personalized to produce a counterfeit.
- Prevents possible secret leakage from manufacturing or ODM sites.
- Eases the manufacturing process, eliminating key or secret injection and key management logistics at the production site, thus saving costs and reducing production time.

5. How can one warn about the reuse of expired parts/accessories?

Each chip has a countdown-only lifespan indicator that can be used to warn or permanently retire any part or accessory. A combination of unique ID, nonvolatile memory data, and lifespan indicator can be used for this purpose as well.

6. Is it cost-effective and easy to implement?

The solution is architected and designed to achieve a balance between cost, degree of security, and ease of implementation. It can meet stringent security requirements while allowing easy implementation with a reasonable cost structure. Infineon provides the code library package that also contains the ECC library, simplifying the implementation process and saving time.

Protection worth the cost

As noted, the goal in designing for counterfeit protection is to achieve an efficient level of security while limiting the impact on the Bill-Of-Materials (BOM) cost. For example, printer cartridge manufacturers and cell phone manufacturers want to protect revenue streams and ensure device reliability.

The software-to-hardware solution described herein addresses the requirements for secure product authentication at a BOM cost – in relatively high product volume, well under one dollar. Additional applications including unique platform identification, remote peripheral authentication and reporting for warranty and services, binding application or firmware to a particular platform, multifactor authentication, and machine-to-machine authentication are also economically viable. With its low-power single-wire implementation, the device is particularly suited for embedded systems. ECD

Robert Rozario *is a technical marketing and application engineering manager for the Chip Card and Security Business Unit at Infineon Technologies. He primarily focuses on Infineon TPM and hardware authentication solutions. Robert holds an MS in Electrical Engineering from the University of Utah.*

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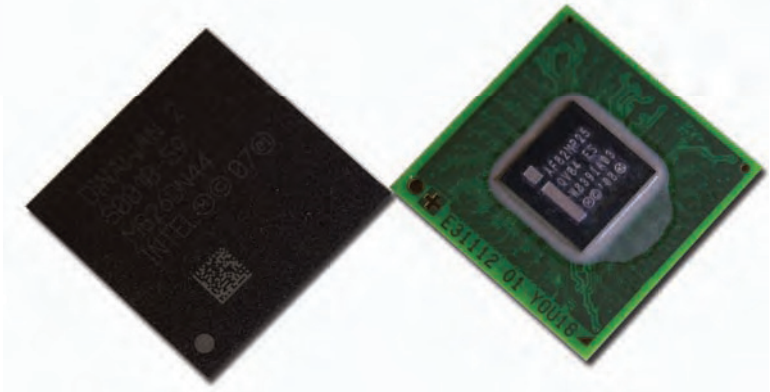
Editor's Choice



Atom, the next generation

This one is an easy choice for me: Intel has rolled out its second-generation Atom processor platform. While I've said that "Tunnel Creek" is a very interesting development, it's still a ways off and targeted for larger devices – tablets, medical and home systems, and more with space for a low-power chipset. The long-awaited "Moorestown" platform is here now, and will soon be mainstream for low-power Intel Architecture designs.

"Moorestown" describes a platform with three parts: the CPU, "Lincroft," now named the Atom processor Z6xx with processor core, 3D graphics and video units, and memory and display controllers; "Langwell," now the PCH MP20, a hub with NAND flash controller, audio, camera, USB, security, wireless and more; and "Briertown," the mixed-signal IC that includes power management.

Intel | www.intel.com
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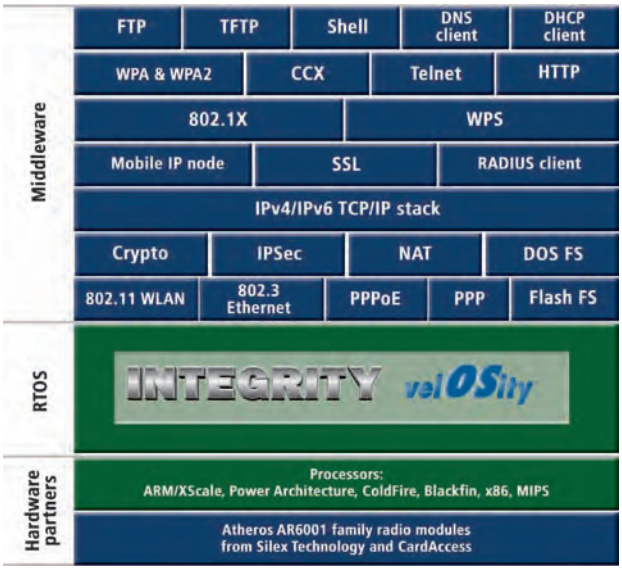
Wi-Fi stacks up

We take Wi-Fi support for granted from a user perspective, but there's a lot that goes into securely building it into a device. The wireless chipset is important, but it's a paperweight without software support. Providing a great example of what can be done, Green Hills Software has recently expanded its Platform for Wireless Devices.

Working with Silex Technology, Green Hills now offers support for Silex's SX-SDCAG 802.11a/b/g SDIO card module based on the Atheros AR6002 wireless chipset. Running on top of INTEGRITY, the wireless functions can be securely and reliably separated from other system functions, and as shown in the block diagram, the platform supports many features and popular Wi-Fi functions like WPA, WPA2, and EAP.



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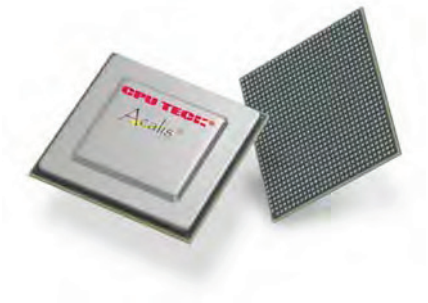

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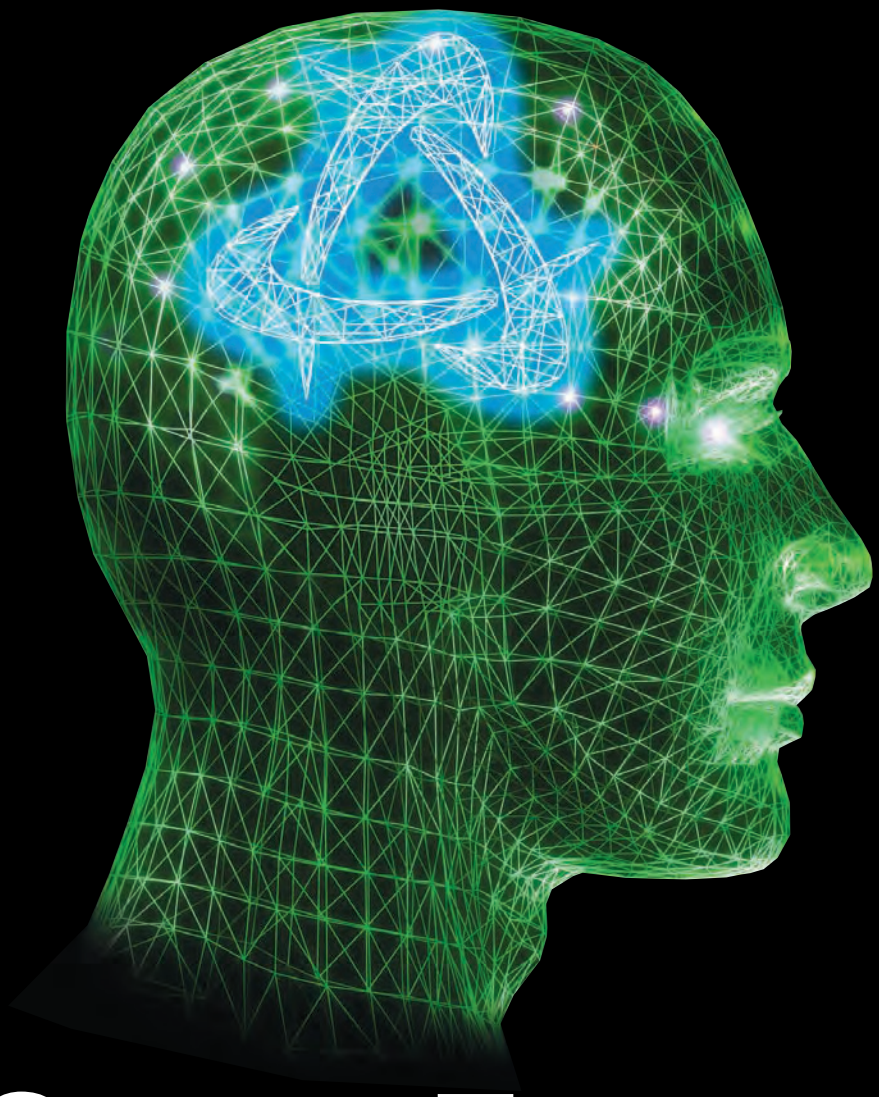

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	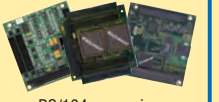	
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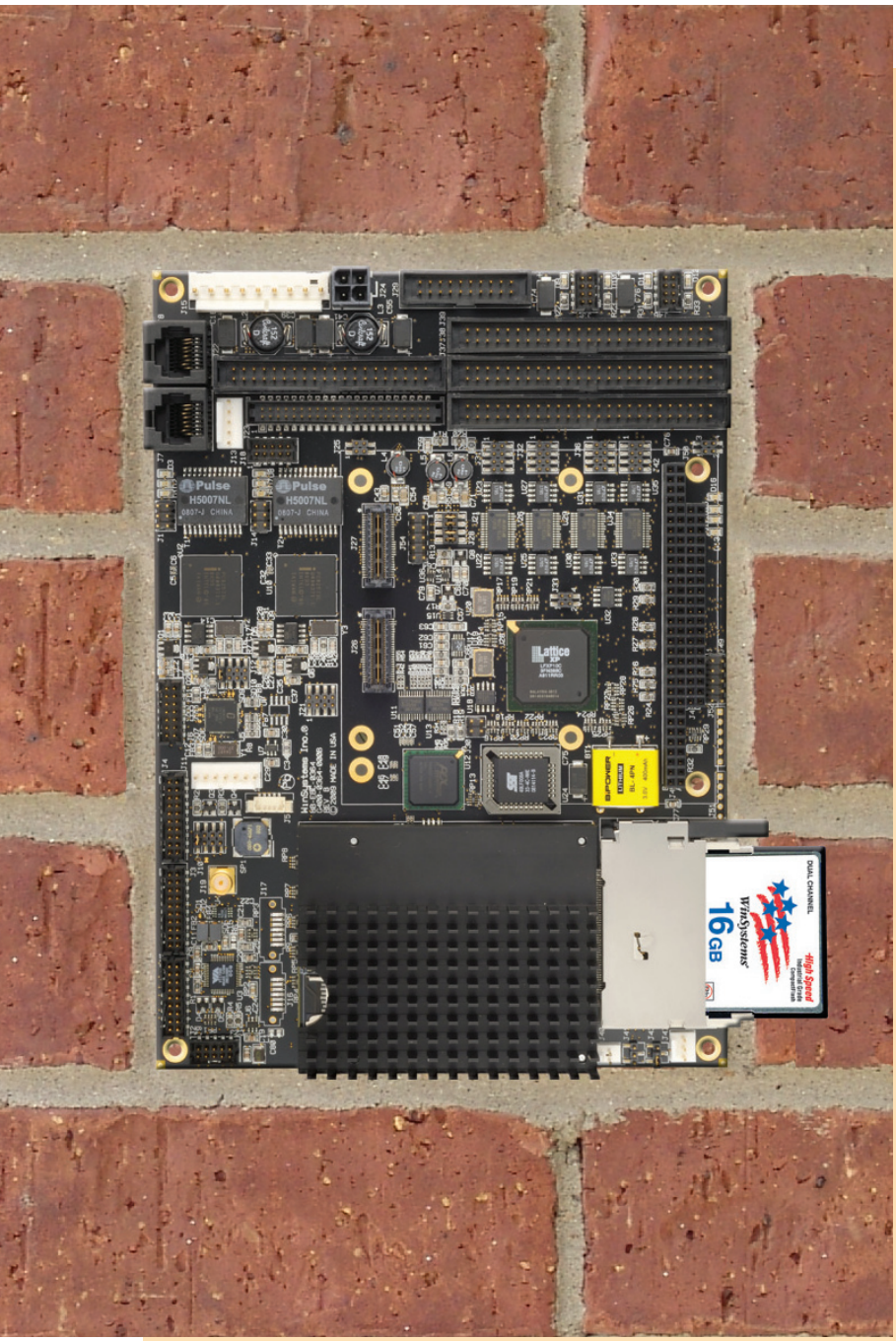
Embedded Solutions for Real World Problems

WinSystems' single board computers and I/O cards provide powerful standard building blocks for embedded systems.



Embedded PCs are the building blocks for industry. As the size, cost, and computing power of embedded computers has plummeted, the number and diversity of applications has exploded. This is due in part to the ability to buy off-the-shelf hardware and development software tools in order to speed prototyping and system integration tasks. The result is that designers spend their time developing new products rather than trying to design yet another proprietary system.

At WinSystems, we handle the complicated, difficult, and time-consuming issues of designing and manufacturing an embedded PC. So you can focus on developing your actual application software, not the scavenger hunt associated with designing, building, and testing a computer from scratch. This modular approach lets you shrink a PC to fit into your product in a very short period of time.

RoHS compliant

Linux

Microsoft Windows Embedded Partner

Extended Temperature

M2M 100 COMPANIES 2010

WinSystems®

When you buy from WinSystems, you are buying more than just a product. You are receiving our company's engineering and manufacturing expertise along with the support of our dedicated professionals. Our staff of trained engineers will assist you in analyzing, configuring, and selecting hardware products while providing you with technical support from initial design into production.

QUALITY BY DESIGN

TECHNOLOGY & INNOVATION

PRODUCT RELIABILITY

LONG TERM COMMITMENTS

OUTSTANDING TECHNICAL SUPPORT

Mew and Sye, two of WinSystems' employee-owners.

Profit from our 28 years of proven experience with our wide selection of Single Board Computers (SBCs), I/O modules, CompactFlash devices, and accessories. Additional product features include extended temperature operation, low power, and two-year warranty. Combined with knowledgeable, award-winning technical support and long-term availability, makes WinSystems' products the right choice for reliable, x86-based embedded PCs.

WinSystems supports and promotes open hardware and software standards. We offer both bus and busless SBCs with SUMIT, PC/104, and Pico-I/O expansion. Plus we also continue to supply legacy STD Bus products.

As you look through this catalog, you will find an overview of our diverse product line. For the most up-to-date technical information, please be sure to visit our Website: http://www.winsystems.com.

We, the employee-owners of WinSystems, look forward to working with you on your next project.

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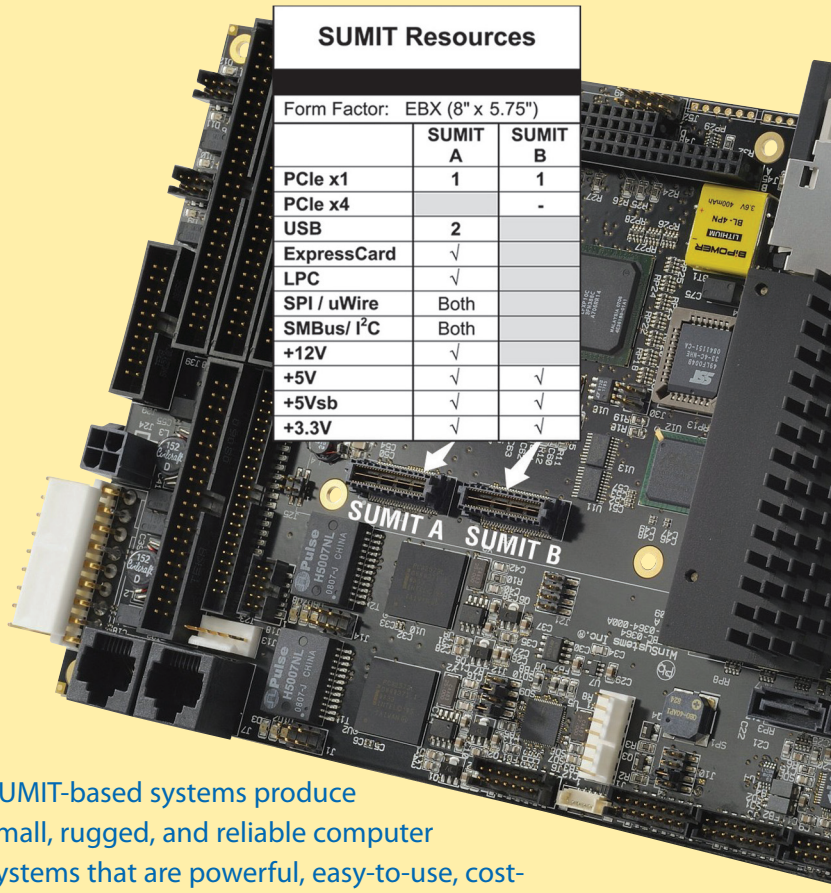
SUMIT TECHNOLOGY

Smaller, faster, low power, and networked; these are the continuing trends of embedded computers. Choosing a small form factor (SFF) board as a system component increases reliability while reducing time-to-market. To meet the needs of higher-performance systems, WinSystems was integral in the development of SUMIT and COMIT.

WinSystems' engineers co-designed SUMIT, a Stackable Unified Modular Interconnect Technology. SUMIT's architecture is I/O-centric and addresses the vast majority of peripherals used by embedded systems using a stacking architecture. It is both form factor and processor independent.

Pronounced "sum it," it is an interconnect standard for embedded systems that uses two, 52-pin, high-density connectors. This interconnect standard integrates the high-speed PCI Express and USB 2.0 serial bus technologies used by the latest generation chipsets, while also providing a bridge to legacy I/O technologies as well.

WinSystems has designed SUMIT-based products for PC/104, EPIC, and EBX form factors while still supporting PC/104-I/O expansion modules. This allows for the graceful migration for PCIe-based PC/104 stacks, while unifying I/O expansion across different form factors.



SUMIT Resources

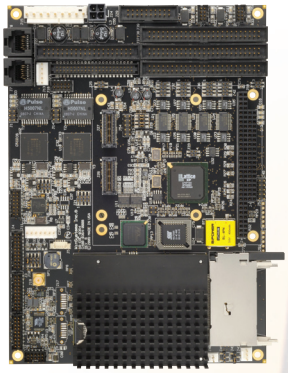
Form Factor: EBX (8" x 5.75")

	SUMIT A	SUMIT B
PCIe x1	1	1
PCIe x4		-
USB	2	
ExpressCard	√	
LPC	√	
SPI / uWire	Both	
SMBus/ I²C	Both	
+12V	√	
+5V	√	√
+5Vsb	√	√
+3.3V	√	√

SUMIT-based systems produce small, rugged, and reliable computer systems that are powerful, easy-to-use, cost-effective, and scalable.

SUMIT A	SUMIT B
One PCI Express x1	One PCI Express x1 & x4 or Five PCI Express x1
Four USB	
LPC (Low Pin Count Bus)	
SPI/uWire	Power
SMBus/I²C Bus	Ground
ExpressCard	Control Signals

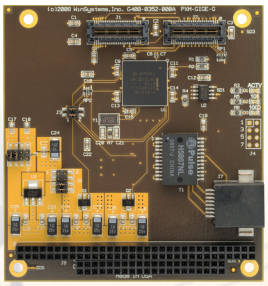
SUMIT Products



Fanless Intel® Atom™ SBC

- Intel® 1.1GHz or 1.6GHz Atom™
- CRT and LVDS flat panel support
- Two Gigabit Ethernet controllers
- Wireless support with MiniPCIe
- 4 COM, 4 USB, and 48 DIO
- LPT port, KYBD, and mouse support
- SUMIT-ISM, PC/104, and Pico-I/O expansion modules
- CompactFlash cards supported
- 5.75" x 8.00" EBX-size board

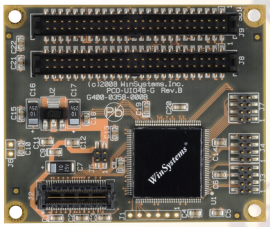
Model: EBC-Z510-G, 1.1GHz
EBC-Z530-G, 1.6GHz



Gigabit Ethernet LAN SUMIT-ISM Module

- Uses 82573 Ethernet controller
- SUMIT x1 PCIe lane
- Gigabit Ethernet controller with automatic switching down to 100 and 10 Mbps
- 90 x 96mm Industry Standard Module
- SUMIT-AB and PC/104 connectors
- RJ-45 connector on board
- Standard Windows® and Linux drivers

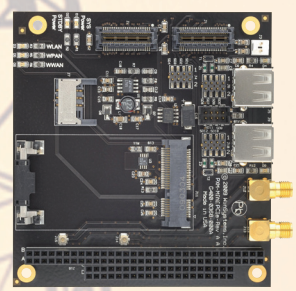
Model: PXM-GIGE



48-Line Digital Pico-I/O Module

- 48 lines programmable for input, output, or output wih readback
- 24 Event sense lines
- TTL compatible I/O
- SUMIT LPC interface requires no BIOS modifications
- -40° to +85°C operation
- Pico-I/O size: 60 x 72mm

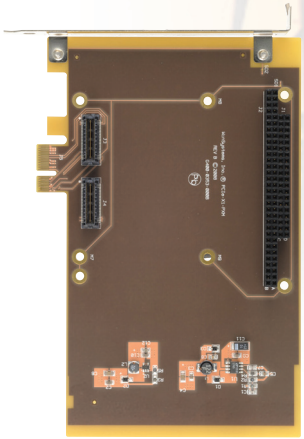
Model: PCO-UIO48



MiniPCIe and USB SUMIT-ISM Module

- SUMIT PCIe x1 interface
- MiniPCIe connector supports wireless, memory, and video modules
- Two USB pass through connectors with overcurrent protection
- PCIe x1 interface to SUMIT
- SUMIT-ISM: 90 x 96mm
- -40° to +85°C operation

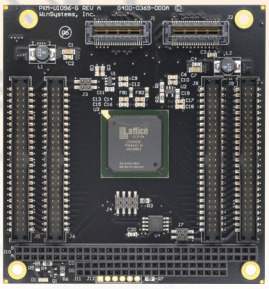
Model: PXM-MiniPCIe



SUMIT-ISM and Pico-I/O PCIe x1 Adapter Card

- I/O module development and debugging for SUMIT-ISM or Pico-I/O cards
- SUMIT-ISM connector adapts PCIe x1 lane into a PCI Express slot
- SUMIT-A and B connectors
- On board power supplies generate both +5V and 5Vsb
- Fits in standard short PCIe card slot

Model: PCIe-x1-PXM



96-Line Digital I/O SUMIT-ISM Module

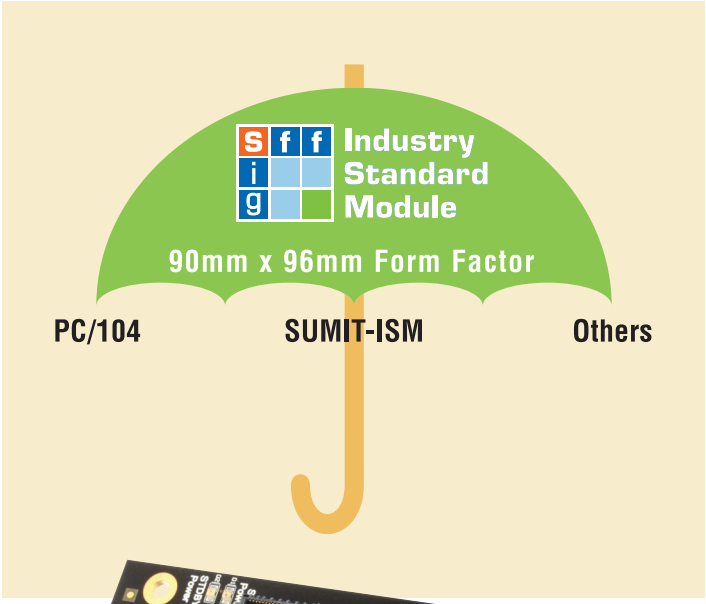
- 96 lines programmable for input, output, or output with readback
- Event sense on change of status
- Direct interface to WinSystems' isolated termination boards
- PCIe x1 interface to SUMIT
- SUMIT-ISM: 90 x 96mm
- -40° to +85°C operation

Model: PXM-UIO96

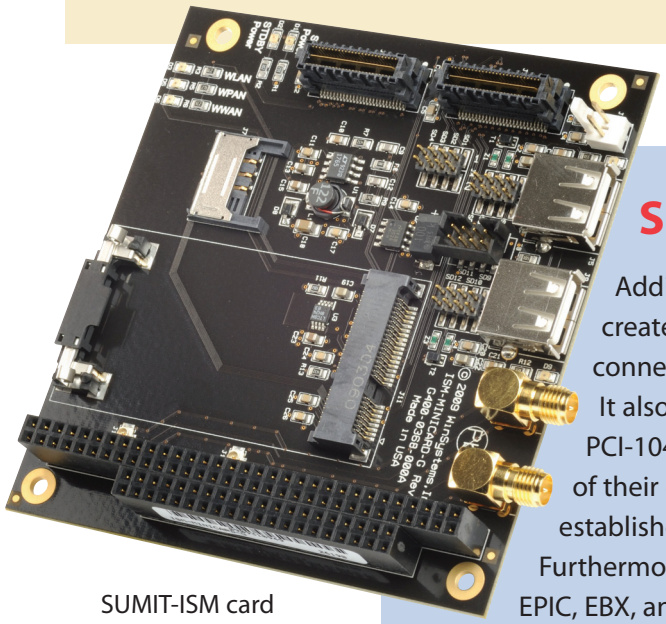
ISM and SUMIT-ISM

Small Form Factor Technology

An Industry Standard Module (ISM) is defined as a 90mm x 96mm form factor board outline without bus expansion. It specifies the board size, four fixed mounting holes, and flexible "expansion zones" for additional circuitry or I/O and/or bus connectors. ISM is an umbrella concept to provide coherence to the many different boards that are available in this 90 x 96mm footprint.



ISM modules are small, easy-to-use, and scalable as they provide a powerful set of building blocks for a variety of different applications. Depending upon the interconnect technology, they can be stacked "piggyback" on top of each other to expand or customize a system solution. This reduces cost and bulk while increasing mounting and packaging options. The best known ISM implementation is PC/104; however, recently SUMIT and other connector configurations have been defined and are being produced as well.



SUMIT-ISM card with legacy PC/104 connector

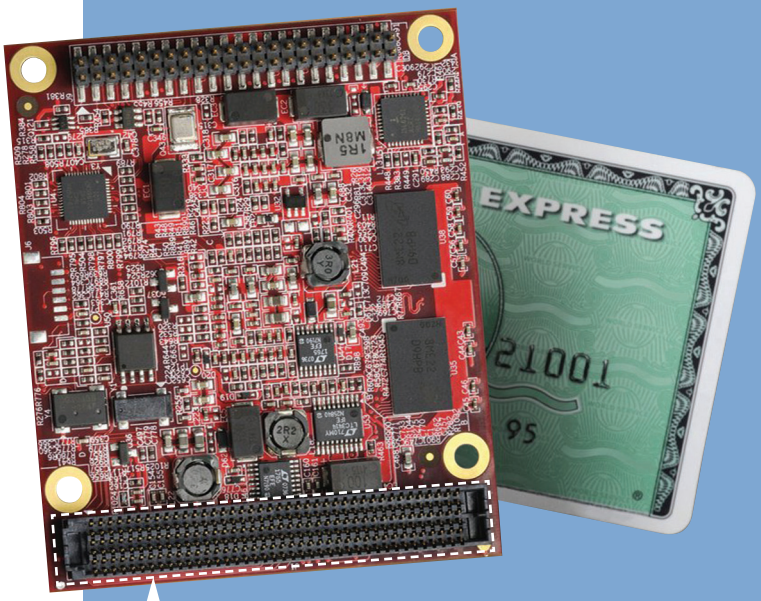
SUMIT + ISM = SUMIT-ISM

Adding SUMIT expansion on the ISM form factor creates SUMIT-ISM. It specifies where the SUMIT AB connectors are located on a 90mm x 96mm module. It also supports a legacy option for PC/104 (Type 1) and PCI-104 (Type 2) modules by allowing the continued use of their connectors in the existing locations plus re-using established physical dimensions and mounting holes. Furthermore, SUMIT-ISM expansion can be supported on EPIC, EBX, and other standard and custom form factors. SBCs using SUMIT-ISM modules allow a designer to build small, reliable, easy-to-use, cost-effective, and stackable systems since they provide a powerful building block for a variety of different applications.

COMIT is a superset of SUMIT Technology

COMIT stands for Computer On Module Interconnect Technology™. COMIT is the enabling technology to allow the design of tiny COM modules to fit within the footprint of industry-standard, small form factor boards such as EBX, EPIC, and PC/104 or other standard or custom-designed motherboards.

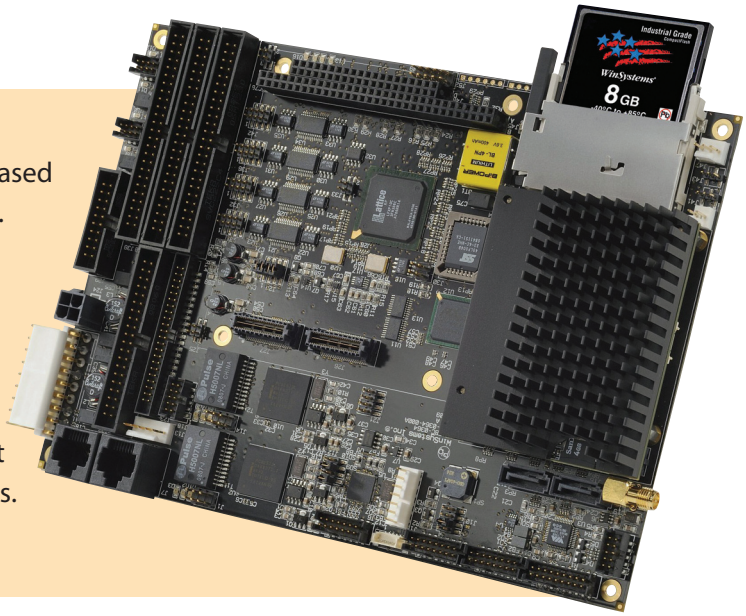
Just as separating the connector and form factor specifications into separate definitions was done in SUMIT, the key differentiation feature of COMIT from other COM specifications is the purposeful exclusion of a myriad of application-specific expansion buses and I/O that are commonly found in other COM architectures. Plus COMIT's high-speed connector will support current and future high-speed signaling for interfaces such as PCI Express Generation 2, Generation 3, USB 3, and SATA600.



COMIT is a 240-pin connector system that supports the most common serial I/O and legacy interfaces from modern chipsets.

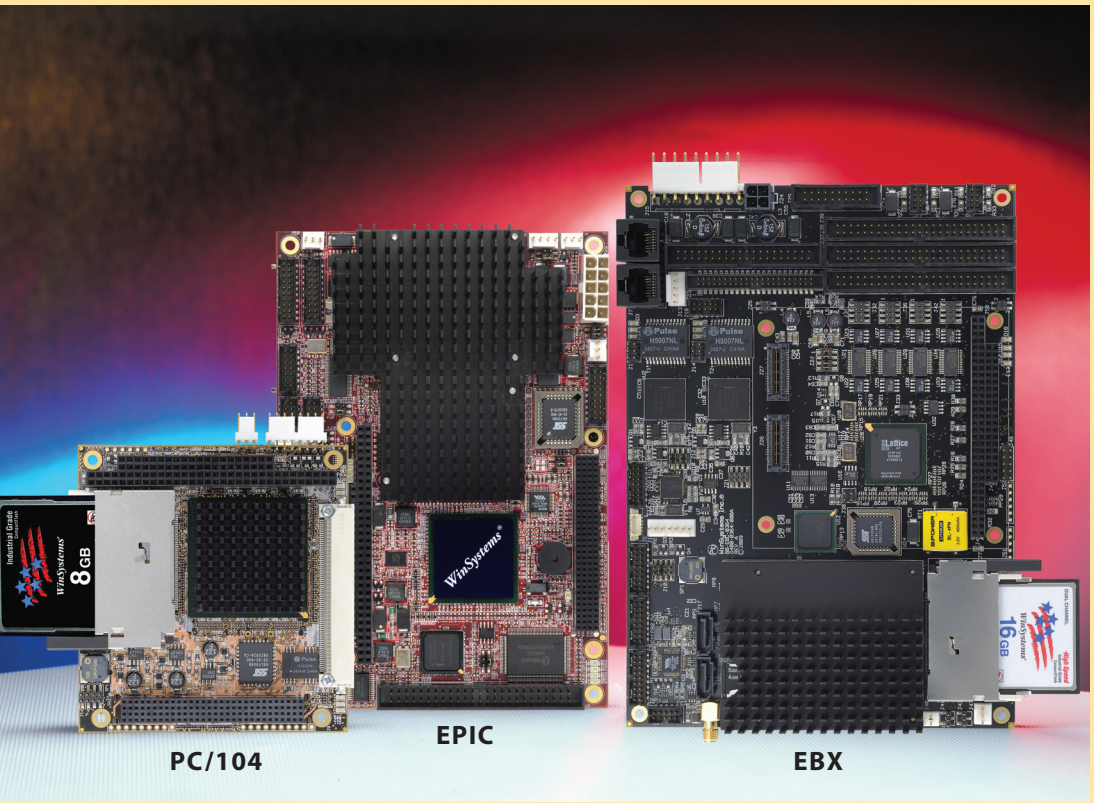
Comit™

WinSystems developed the first COMIT-based SBC that uses the Intel® ATOM™ processor. It is an I/O rich, EBX-sized board that is perfect for applications such as industrial control, medical, security, transportation, communication, and Mil/COTS. Plus this board also has SUMIT and PC/104 connectors to support more I/O expansion with SUMIT-ISM cards.



SINGLE BOARD COMPUTERS

Our Embedded PCs come in three sizes from an industry standard 3.6" x 3.8" module to a 8.0" x 5.75" EBX with SUMIT and PC/104 expansion.

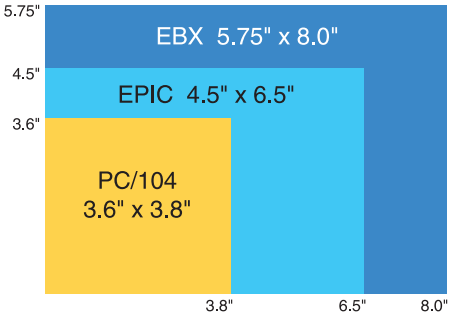


- x86 Compatible
- Compact & Modular
- Rugged & Reliable
- Easy to use
- Extended temperature
- Wide Selection of I/O
- SUMIT, Pico-I/O, and PC/104 Expandable
- 30-day Product Evaluation Program

Small size, low power, wide operating temperature, and PC-compatibility are the fundamental computer elements required for embedded designs. Our feature-rich SBCs meet these requirements and are ideal for space- and power-limited applications in harsh environments.

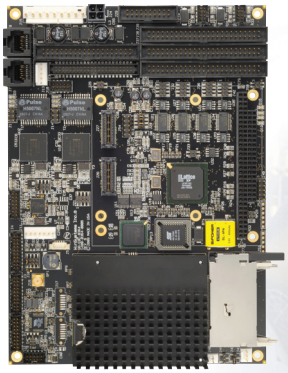
Designed to run x86 instruction set software, these SBCs are compatible with Microsoft's® Windows® operating systems as well as the applications that run on them. They also support Linux, ROM-DOS, and other PC-compatible x86 operating systems. PC software compatibility assures faster program development, debugging, and checkout of your application's software.

A comprehensive SBC selection guide is located on pages 10 and 11.



Size Comparison
PC/104 vs EPIC vs EBX

Single Board Computers

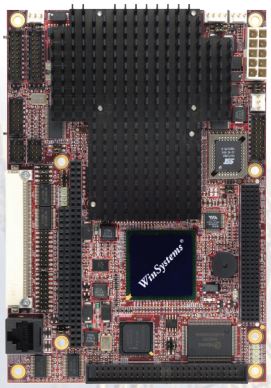


Fanless Intel® Atom™ SBC

- Intel® 1.1GHz or 1.6GHz Atom™
- CRT and LVDS flat panel support
- Two Gigabit Ethernet controllers
- Wireless support with MiniPCIe
- 4 COM, 4 USB, and 48 DIO
- LPT port, KYBD, and mouse support
- SUMIT-ISM, PC/104, and Pico-I/O expansion modules supported
- CompactFlash socket
- 5.75" x 8.00" EBX-size board

Model:

EBC-Z510-G, 1.1GHz
EBC-Z530-G, 1.6GHz

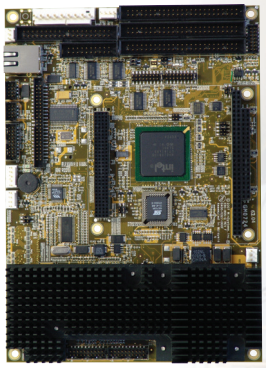


Intel® Pentium® EPIC SBC

- 1GHz or 1.8GHz Intel® CPU
- CRT and LVDS flat panel support
- Gigabit and 10/100 Mbps Ethernet
- 802.11a/b/g wireless available
- 4 COM, 4 USB 2.0, and 24 digital I/O
- LPT port keyboard and FDC I/F
- CompactFlash socket
- PC/104 and PC/104-*Plus* expansion
- 4.5" x 6.5" EPIC-compliant

Model:

EPX-855-G-1G-0, 1.0GHz
EPX-855-G-1G-1, 1.0GHZ with fan
EPX-855-G-1.8G-1, 1.8GHZ with fan

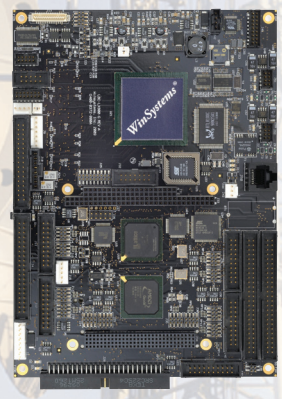


Intel® Pentium® EBX SBC

- 1GHz or 1.8GHz Intel® CPU
- CRT and LVDS flat panel support
- 10/100 Mbps Ethernet controller
- 802.11a/b/g wireless available
- 4 serial COM ports and 4 USB ports
- 48 bi-directional TTL digital I/O lines
- EIDE, LPT, KYBD, and mouse support
- CompactFlash socket
- PC/104 and PC/104-*Plus* expansion
- 5.75" x 8.00" EBX-size board

Model:

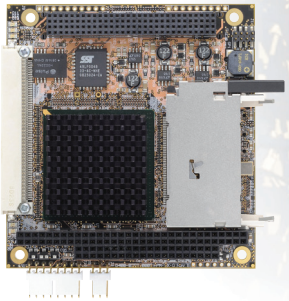
EBC-855-G-1G-0, 1.0GHz
EBC-855-G-1G-1, 1.0GHz with fan
EBC-855-G-1.8G-1, 1.8GHz with fan



All-in-One Fanless SBC

- AMD LX800 CPU
- CRT and LVDS flat panel support
- 10/100 Mbps Ethernet controller
- 12 COM and 4 USB ports
- 48 bi-directional digital I/O lines
- IDE, FDC, keyboard, and mouse support
- CompactFlash socket
- PC/104 expansion connectors
- OEM configurations available
- 5.75" x 8.00" EBX-size board
- -40° to +85°C operation

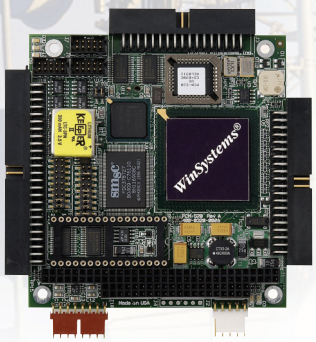
Model: LBC-LX800-G



PC/104-*Plus* SBC with Ethernet and Video

- AMD LX800-based SBC
- CRT and LVDS flat panel support
- Custom splash sceen on start-up
- 10/100 Mbps Ethernet controller
- 4 COM channels and 2 USB
- 16 digital I/O lines with event sense
- LPT, mouse, CF, audio, and IDE interfaces
- PC/104 size: 90mm x 96mm
- -40° to +85°C operation

Model: PPM-LX800-G



SC520-based PC/104 SBC

- 133MHz SC520-based SBC
- Supports CFlash cards
- 10/100 Mbps Ethernet controller
- 4 serial COM ports
- LPT, IDE, and floppy disk interfaces
- PC/104 expansion connector
- Low power, +5V only
- -40° to +85°C operation

Model: PCM-SC520-G

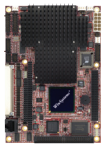
WinSystems' SBC Selection Guide

WinSystems' SBCs are designed for embedded applications and will operate without a rotational disk, keyboard, or a monitor over extended temperature ranges without the need of a fan. They are available in various physical sizes and CPUs to match your application's requirements.

	 EBC-Z530-G	 EBC-Z510-G	 EBC-855-G-1.8G-1	 EBC-855-G-1G-0	 EPX-855-G-1.8G-1
Form Factor	EBX: 5.75" x 8.0"	EBX: 5.75" x 8.0"	EBX: 5.75" x 8.0"	EBX: 5.75" x 8.0"	EPIC: 115 x 165mm
CPU Type	Intel Atom	Intel Atom	Intel Pentium M	Intel ZC Dothan	Intel Pentium M
CPU Speed	1.6GHz	1.1GHz	1.8GHz	1.0GHz	1.8GHz
Chipset	US15W SCH	US15W SCH	855 GME	855 GME	855 GME
System Memory	512 MB soldered	512 MB soldered	Up to 1GB in a socket	Up to 1GB in a socket	Up to 1GB in a socket
Power Management	✓	✓	✓	✓	✓
CompactFlash Socket	✓	✓	✓	✓	✓
VGA	✓	✓	✓	✓	✓
LCD	✓	✓	✓	✓	✓
LVDS	✓	✓	✓	✓	✓
Custom Splash Screen	✓	✓	✓	✓	✓
Simultaneous Video	✓	✓	✓	✓	✓
10/100/1000 Ethernet	2	2	1	1	1
10/100 Ethernet	–	–	–	–	1
USB 2.0 Ports	4	4	4	4	4
RS-232/422/485	4	4	2	2	2
RS-232 Only	–	–	2	2	2
Digital I/O	48	48	48	48	24
EIDE Interface	2	2	2	2	2
SUMIT Connector	AB	AB	–	–	–
PC/104 Connector	–	✓	✓	✓	✓
PC/104-*Plus* Connector	✓	–	✓	✓	✓
Mini PCIe Socket	✓	✓	–	–	–
Mini PCI Socket	–	–	✓	✓	✓
Mouse	PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB
LPT	✓	✓	✓	✓	✓
Keyboard	PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB
Audio	HD	HD	AC97	AC97	AC97
Fanless	✓	✓	–	✓	–
Ex. Temp. Operation	-40°C to +60°C	-40°C to +70°C	-40°C to +70°C	-40°C to +70°C	-40°C to +70°C
Power Supply	+5	+5	+5	+5	+5
Battery Onboard	Opt.	Opt.	Opt.	Opt.	Opt.

Software

WinSystems' x86-compatible single board computers run Linux, Windows® XP embedded, ROM-DOS, and other compatible RTOSs along with their development tools. Each of our SBCs and I/O boards comes with free software drivers.

 EPX-855-G-1G-0	 LBC-LX800-G	 LPM-LX800-G	 PPM-LX800-G	 PCM-SC520-G	
EPIC: 115 x 165mm	5.75" x 8.0"	STD Bus: 4.5" x 6.5"	PC/104-*Plus*: 90 x 96mm	PC/104: 90 x 96mm	Form Factor
Intel ZC Dothan	AMD LX800	AMD LX800	AMD LX800	AMD SC520	CPU Type
1.0GHz	500 MHz	500 MHz	500 MHz	133 MHz	CPU Speed
855 GME	CS5536	CS5536	CS5536	–	Chipset
Up to 1GB in a socket	Up to 1GB in a socket	Up to 1GB in a socket	Up to 1GB in a socket	Up to 256MB in a socket	System Memory
✓	–	–	–	–	Power Management
✓	✓	✓	✓	✓	CompactFlash Socket
✓	✓	✓	✓	–	VGA
✓	✓	✓	✓	–	LCD
✓	✓	✓	✓	–	LVDS
✓	✓	✓	–	–	Custom Splash Screen
✓	✓	✓	✓	–	Simultaneous Video
1	–	–	–	–	10/100/1000 Ethernet
1	1	1	1	1	10/100 Ethernet
4	4	2	2	–	USB 2.0 Ports
2	12	2	2	2	RS-232/422/485
2	–	2	2	2	RS-232 Only
24	48	48	16	–	Digital I/O
2	1	1	1	1	EIDE Interface
–	–	–	–	–	SUMIT Connector
✓	✓	✓	✓	✓	PC/104 Connector
✓	✓	✓	✓	–	PC/104-*Plus* Connector
–	–	–	–	–	Mini PCIe Socket
✓	–	–	–	–	Mini PCI Socket
PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB	Mouse
✓	✓	✓	✓	✓	LPT
PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB	PS/2 or USB	Keyboard
AC97	AC97	AC97	AC97	–	Audio
✓	✓	✓	✓	✓	Fanless
-40°C to +70°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	Ex. Temp. Operation
+5	+5	+5	+5	+5	Power Supply
Opt.	Opt.	✓	Opt.	✓	Battery Onboard

PC/104 MODULES

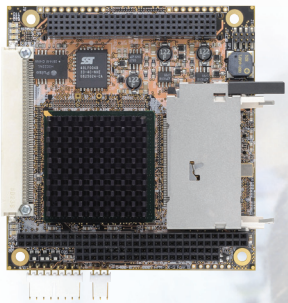
Small, stackable SBC and I/O modules are building blocks for embedded systems.

PC/104 modules are small, reliable, easy-to-use, cost-effective, scalable, and powerful computer components used in a variety of industrial applications. PC/104 is simply the desktop PC modularized, repackaged, and hardened for industrial use. These 90mm x 96mm modules are nearly the size of a 3.5-inch floppy disk.

Modules are available as SBCs or specialty I/O for configuration flexibility and application-specific needs. PC/104 boards can be used as standalone units, stacked one on top of another, or stacked on a larger SBC in a mezzanine fashion. Most WinSystems' modules operate over an extended temperature range of -40° to +85° Celsius.

Bob Burckle
Vice President

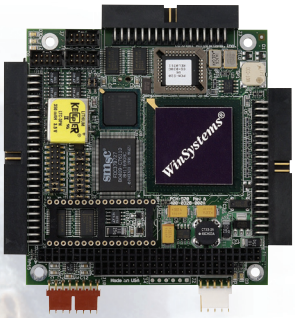
PC/104 SBCs and Panel PC



Ethernet and Video PC/104-*Plus* SBC

- AMD LX800 SBC
- x86 software compatible
- Video with CRT resolutions to 1920 x 1440 and panel resolutions to 1600 x 1200
- Custom splash screen on start-up
- Up to 1 GB of SDRAM
- 10/100 Mbps Ethernet controller
- Four COM channels with FIFOs
- Two USB 2.0 with overcurrent protection
- 16 digital I/O lines with event sense
- LPT, Mouse, CF, audio and IDE interfaces
- PC/104-*Plus* compliant
- -40° to +85°C operation

Model: PPM-LX800-G

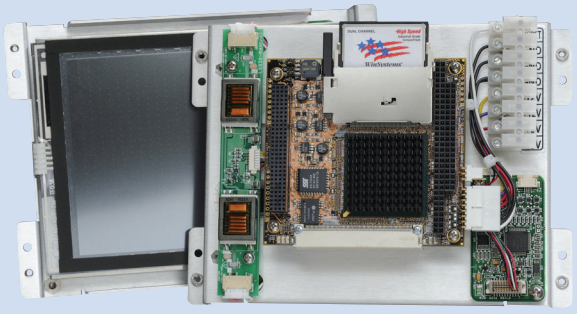


SC520-based PC/104 SBC

- 133MHz SC520-based SBC
- Fully x86 software compatible
- Up to 256MB of SDRAM
- Supports up to 16GB of CFlash
- 10/100 Mbps Ethernet controller
- Four serial COM ports with FIFOs
- LPT, IDE and floppy disk interfaces
- Watchdog timer and RTC
- 16-Bit PC/104 bus expansion
- Mouse and AT keyboard supported
- PC/104 compliant
- Low power, +5V only
- -40° to +85°C operation

Module: PCM-SC520-G

6.5-inch PC/104 Flat Panel Computer

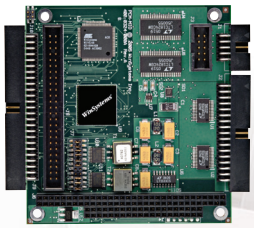


Model: PPC3-6.5

The compact PPM-LX800 PC/104-*Plus* SBC supplies the computing power for the PPC3 open frame 6.5- inch Panel PC. This light-weight, integrated system combines flat panel display, SBC, and touchscreen into an industrial-grade, open-frame enclosure that is less than two inches thick.

Ready-to-mount in harsh environments, its PC-compatibility supports Linux and Windows® XP embedded, along with real-time kernels. It operates over an extended temperature from -20° to +70°C.

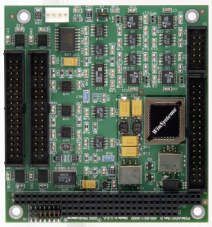
PC/104 Analog and Digital I/O



Multifunction Analog and Digital I/O

- Two, 16-bit A/D converters with 0-5V, 0-10V, ±5V, and ±10V
- Up to 16 SE and 8 DI channels
- Speed: 100K samples/sec
- Eight, 12-bit D/A converters
- 48 lines of digital I/O
- -40° to +85°C operation

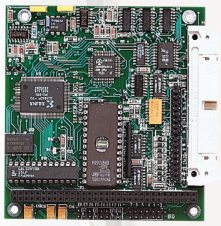
Model: PCM-MIO



12-Bit Analog I/O

- 8 channel, 12-bit A/D: 0 to +5V or ±2.5V
- 100KHz sampling rate
- SE or DI uni- or bipolar
- Two 12-bit D/A channels: 0 to +5V or ±5V
- Windows®, Linux, and C drivers
- -40° to +65°C operation

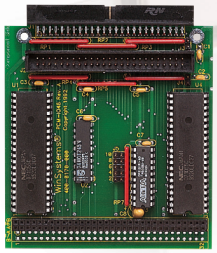
Model: PCM-ADIO



Smart Sensor Module

- 8 channel, 16-bit A/D resolution
- Supports thermocouples, RTDs, strain gauges, voltage inputs, 4-20mA loops, and thermistors
- Self-calibration eliminates need for adjustment
- -25° to +85°C operation

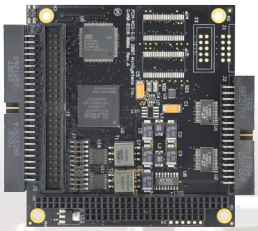
Model: PCM-518



Digital I/O

- 48 digital I/O lines
- Two 82C55A PPIs
- Dual 50-pin connectors
- Interfaces to two, Opto-22 (or equiv) module racks
- +5V only operation
- -40° to +85°C operation

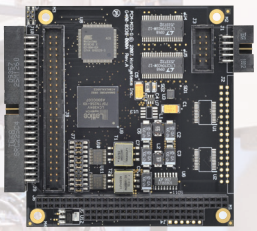
Model: PCM-IO48



Analog Input and Digital I/O Module

- Two, 16-bit A/D converters with 0-5V, 0-10V, ±5V, and ±10V
- Up to 16 SE and 8 DI channels
- Conversion speed: 100K samples/sec
- 48 lines of digital I/O
- -40° to +85°C operation
- No calibration required

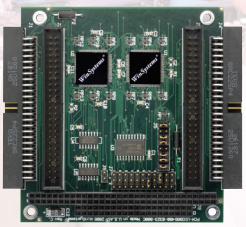
Model: PCM-MIO-AD



Analog Output and Digital I/O Module

- Eight, 12-bit D/A converters with 0-5V, 0-10V, ±5V, and ±10V
- No calibration required
- 48 lines of digital I/O
- 12 mA sink current per line
- Windows®, Linux, and C drivers
- -40° to +85°C operation

Model: PCM-MIO-DA



96-Line I/O with Event Sense

- 96 lines as input, output, or output with readback
- 48 of the lines can generate interrupt requests that are edge selectable, latched and software enabled
- 12 mA sink current per line
- -40° to +85°C operation

Model: PCM-UIO96A

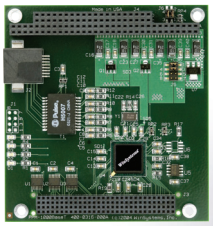
48-Line I/O with Event Sense

- 48 lines as input, output, or output with readback
- 24 of the lines can generate interrupt requests that are edge selectable, latched and software enabled
- 12 mA sink current per line
- -40° to +85°C operation

Model: PCM-UIO48A

Boards stocked for quick availability...Call 817-274-7553.

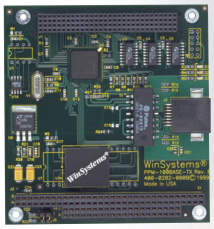
PC/104 Communication



Gigabit Ethernet Controller

- Gigabit PCI Ethernet controller
- Auto-switching from 1Gbps thru 100 and 10 Mbps
- Full- and half-duplex operation
- IEEE 802.3ab Auto-Negotiation support
- RJ-45 connector on the board
- PC/104-*Plus* module
- -40° to +85°C operation

Model: PPM-GIGABIT



Fast Ethernet Controller

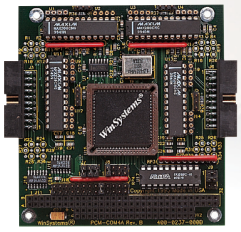
- IEEE 802.3 10BASE-T and 100BASE-TX compatible 100 Mbps
- Full- or half duplex at 10 or 100 Mbps
- Fast Ethernet PCI controller
- RJ-45 Ethernet interface connector
- Adaptive equalization supported
- -40° to +85°C operation

Model: PPM-10/100

Octal Serial I/O

- Eight independent COM channels
- Two 16C554-compatible quad UARTs support RS-232/485/422 levels
- 128byte Rx and Tx FIFOs
- Data rates to 115,200bps
- All outputs short circuit protected
- +5V only operation
- -40° to +85°C operation

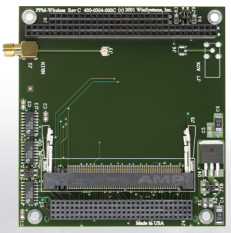
Model: PCM-COM8



Quad Serial Module

- Four RS-232 COM ports
- Optional RS-422/485 on each channel
- 16C554 UART with 16-byte Tx and Rx FIFOs
- Data rates to 115,200bps
- +5V only operation
- -40° to +85°C operation

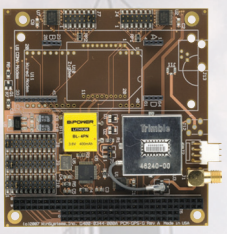
Model: PCM-COM4



Wireless 802.11 Adapter

- IEEE 802.11 wireless adaptercard
- Supports 802.11 miniPCI modules
- Available with or without a card installed
- External antenna connector
- PC/104-*Plus* module
- -40° to +85°C operation

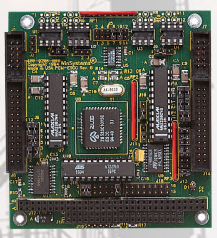
Model: PPM-WIRELESS



GPS Receiver

- GPS receiver board
- 12 channel simultaneous operation
- Dual sensitivity modes w/auto-switching
- TSIP, TAIP, and NMEA 0183 supported
- Pulse output for accurate time standard
- Programmable address and interrupt settings
- -40° to +85°C operation

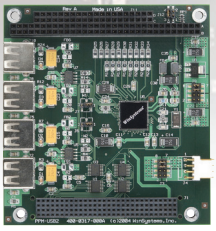
Model: PCM-GPS



Dual Synchronous Serial Controller

- Uses 85230 ESCC
- Two full-duplex, independent
- RS-232 channels with FIFO
- Supports Async, X.25, HDLC, SDLC, and BISYNC
- DMA supported
- -40° to +85°C operation
- +5V only operation

Model: PCM-ESCC

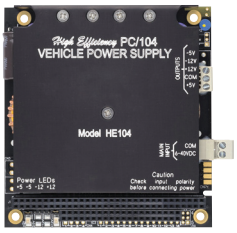


Four-channel USB 2.0 Module

- OHCI host and EHCI Host Compliant
- Root hub and 4 downstream facing ports onboard
- All downstream ports handle low-speed, full-speed, and high-speed transactions
- Each port with overcurrent and in-rush protection
- PC/104-*Plus* module
- -40° to +85°C operation

Model: PPM-USB2

PC/104 Expansion



High Efficiency Power Supply

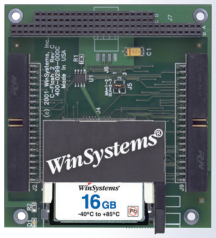
- 50W DC/DC power supply
- Input ranges: 6V to 40V
- Output: +5V @ 10A, +12V @ 2A
- Low output ripple
- Voltage status LEDs
- Quick disconnect connector
- -40° to +85°C operation

Model: PCM-HE104

Single Slot PC Card & Cardbus Adapter

- Supports 802.11 a/b/g, Bluetooth, 1394 Firewire, USB 2.0 PC cards
- Provides 33MHz PCI performance
- Hot insertional and removal support
- Accommodates both 5V/3.3V PC cards
- Low power required
- Single +5V supply

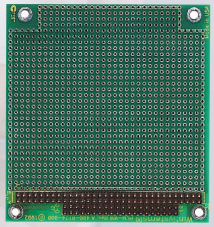
Model: PPM-Cardbus



CompactFlash Disk Adapter Module

- CF Type I or II interface to IDE
- Compatible with Windows and Linux
- On-card automatic power management
- Supports multiple drive operation
- Remote mounting configuration available
- -40° to +85°C operation

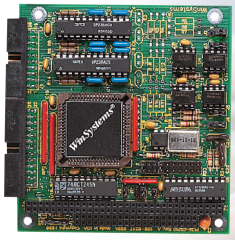
Model: PCM-CFlash2



Prototyping Module

- 16- or 8-bit universal prototyping module
- Access to all PC/104 lines and power buses
- Breadboard area on 0.100" grid accepts DIP sockets, connectors, and logic
- -40° to +85°C operation

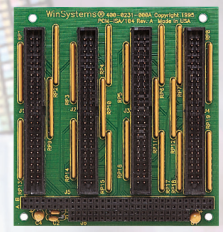
Model: PCM-WW



Dual COM & LPT

- One LPT printer port
- Two RS-232 COM ports with RS-422/485 on each channel
- 16C552 UART with 16-byte Tx and Rx FIFOs
- Date rates to 115, 200bps
- +5V only operation
- -40° to +85°C operation

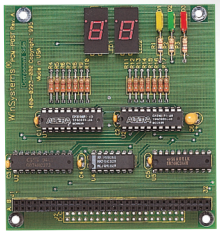
Model: PCM-DSPIO



PC/104 to ISA Bus Adapter

- High speed, low cost adapter transfers data at system clock speeds with no WAIT states
- Direct bus-to-bus interface
- No configuration switches
- Easy-to-use
- Links two bus architectures

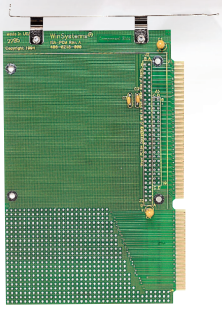
Model: PCM-ISA



POST Module

- System diagnostic tool
- BIOS POST codes shown on two 7-segment displays
- Supports user diagnostic and status codes
- LEDs provide visual status of power supplies
- -40° to +85°C operation

Model: PCM-POST



ISA to PC/104 Adapter

- Half-size ISA Bus card accepts PC/104 module plugged into an ISA slot
- Direct bus-to-bus interface
- "In Systems Emulation" for quick-program development
- Wire-wrap area on board

Model: ISA-PCM

Check out our website...www.WinSystems.com

Quick Start Kits and Enclosures

- Integrated bench-top chassis provides easy access to WinSystems SBCs
- Preloaded with DOS, Linux, or Windows® XPe sample image
- Supports 3.5" floppy disk, removable IDE drive and one DVD drive
- Includes POST card, memory, CFlash
- Light-weight aluminum construction with black powder coat finish
- Power supply included

Quick Start Kits

Small Form Factor Board Enclosures

- Enclosures for PC/104, EPIC, and EBX form factors
- SBC mounting plate with standoffs
- Room for cable runs inside the box
- Standard or user-configuration end plates
- Slotted keyways for easy mounting
- Lightweight aluminum is strong but will not rust
- Black powder coat finish
- Designed for easy assembly
- Custom end plates at moderate volumes
- RoHS compliant

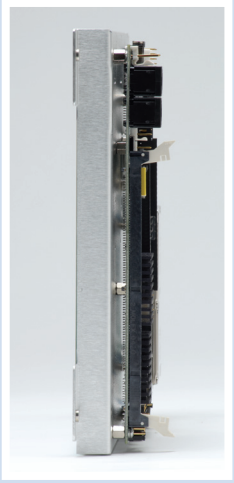
Open Frame Panel PCs

WinSystems' Panel PCs support Linux and Windows® XP embedded plus real time kernels.

WinSystems' 6.5-, 12.1, and 15-inch open-frame Panel PCs (PPCs) provides crisp image quality for HMI industrial applications. A PPC includes a color TFT flat panel display, PC-compatible SBC with Ethernet and touchscreen integrated into an open-frame enclosure.

The combination of embedded PC functionality and industrial-grade construction makes these units ideal for industrial automation and control applications with tight system integration and minimal space requirements. A PPC will operate over the temperature range of -20° to +70°C.

Each PPC's SBC has an ample amount of I/O support onboard. More I/O is available with wired or wireless Ethernet, USB, or PC/104 expansion modules.



- Includes a PC-compatible single board computer (SBC) mounted with PC/104 I/O module expansion capability
- Active Matrix color LCD with touch screen
- Thin profile, small size
- Industrial-grade resistive touch screen
- Easy to mount, open-frame design
- Rugged and reliable construction
- Gasket material supplied for better fit into application enclosure
- Extended temperature operation
- Plus award-winning technical support

30-day product evaluations available.

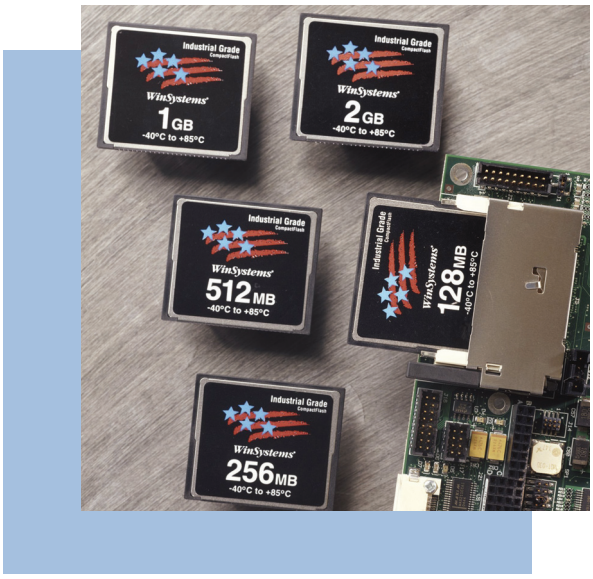
Industrial CompactFlash

WinSystems specializes only in CompactFlash devices that operate over the entire industrial temperature range of -40°C to +85°C.

They support static and dynamic wear leveling to insure long life plus error correction and detection on the data.

- 128MB to 16GB storage capacity
- Up to 66MB/s (burst) with 37MB/s Read and 16MB/s Write (sustained)
- Sophisticated error checking and wear leveling
- Withstands 2000 G's shock and 16.3 G's of vibration
- -40°C to +85°C operating temperature
- Knowledgeable engineering phone support
- In-stock availability and RoHS compliant

These industrial-grade CF cards have higher reliability, longer endurance, lower-power consumption, and more powerful performance over their commercial-grade counterparts. They are designed and manufactured for use in harsh and rugged applications that are mission critical.



WinSystems offers both standard and high-speed dual channel industrial CompactFlash cards. Both are designed to serve the communications, networking, transportation, utility, industrial, server/storage, military/aerospace, medical, security, and surveillance markets.

Extended Temperature

CFA

RoHS compliant

STD BUS OVERVIEW

Here Today, Here Tomorrow

- Worldwide standard IEEE 961
- Open architecture
- Modular
- Small Size
- High Reliability
- Ruggedness
- Serviceability
- Easy to Use
- Continued Availability

Jerry Winfield
President

WinSystems' Long-Term Commitment

We continue to support the STD Bus after 30 years since our customers still want products.

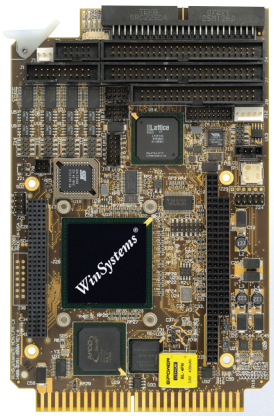
Referred to as the "Blue Collar Bus" because of its well-proven design and small size, the STD Bus is designed for the factory and industrial environments.

Our engineers designed the original STD Bus microprocessor and I/O boards. We continue to be a dependable, long-term supplier of STD Bus products.

As an established STD Bus manufacturer, we also have over 100 replacement boards for other manufacturers such as Pro-Log/ Motorola, Analog Devices, and Mostek/Mizar to name a few.

We offer a 30-day trial evaluation period for our plug-in replacement cards. This program provides a cost-effective option when price, delivery, and continued support are critical issues.

STD Bus Products



SBC with Video, Ethernet, and I/O

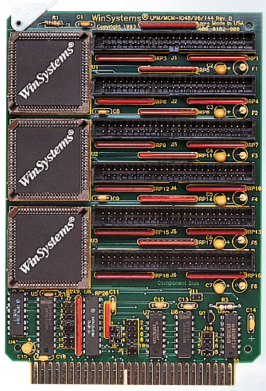
- AMD LX800 MHz 0.9W CPU
- Up to one Gigabyte of SDRAM
- LCD and CRT supported
- Custom splash screen on start-up
- 10/100Mbps Ethernet controller
- 4 USB and 4 COM ports
- 48 digital I/O lines plus LPT
- Audio, CF, IDE and Mouse interfaces
- PC/104-*Plus* expansion connectors
- -40° to +85°C operation

Model: LPM-LX800-G

Card Cages and Powered Racks

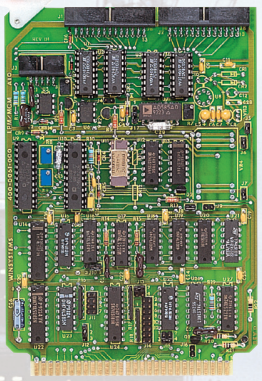
- From 2 to 26 card slots
- 0.75″ or 0.625″ spacing
- Rack, Table, or Wall mount configurations
- 50W or 100W power supplies
- Standalone backplanes
- Rugged construction
- Voltage status LEDs
- Extended temperature operation

Model: CC and CX Series



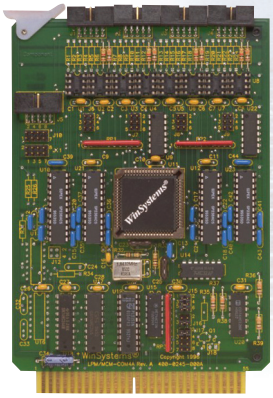
Digital I/O Cards

- 144-, 96- or 48-line digital I/O with interrupt on change-of-state
- 48-line isolated relay driver card
- 48-channel debounced isolated input card with selectable polarity
- Extender and wire-wrap cards
- -40° to +85°C operation available
- Live telephone engineering support



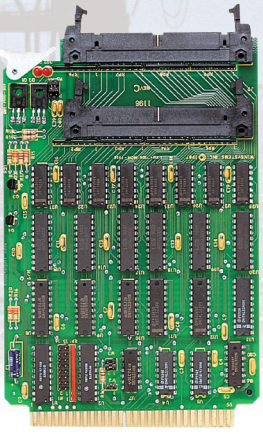
Analog I/O Cards

- 16 SE/8 DI 12-bit input channels with 0-5V, 0-10V, ±5V, and ±10V range
- Eight, 12-bit output channels with 0-5V, 0-10V, ±5V, and ±10V range
- 12-bit combination Analog I/O card
- Optional DC/DC converters
- Extended temperature operation



Communication Cards

- Dual and Quad COM cards
- RS-232/422/485 support
- TX and RX FIFOs
- Data rates to 115.2 Kbps
- +5V only operation
- Optional -40° to +85°C operation
- Live telephone engineering support



Legacy CPU and I/O Products

- Analog, Digital, Serial, Parallel, and Communication I/O Modules
- Substitutes for Pro-Log, DY-4, and Mostek/Mizar products
- Knowledgeable technical support
- 30-day product evaluation
- STD or CMOS STD Bus

ABOUT WINSYSTEMS

WinSystems builds strong business relationships with our customers by providing high-quality, cost-effective products along with extraordinary customer service.

Service *Responsiveness* *Knowledge* *Quality* *Trust*

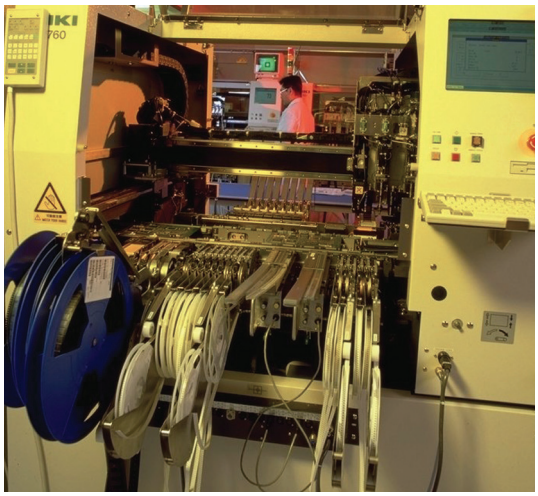
WinSystems is a leading provider of embedded products for use in industrial environments. Founded in 1981, we have been in business over 28 years and are an employee-owned, solid company.

Our facilities are located in a 55,000 square foot office campus. This houses our design, manufacturing, and support teams as well as our corporate headquarters. We are located in Arlington, Texas, midway between Dallas and Fort Worth.

We have made a major capital investment in both our facilities and inventories. We purchase our own components to assure that they are qualified for use on our boards. We also maintain both a sizeable in-house parts inventory and finished goods

stock. All parts are selected for long term availability plus monitored for their continued status.

We have two surface mount production lines in-house capable of handling fine-pitch and ball grid technology. This includes automatic pc board feeders, pick-and-place machines, reflow ovens and wash systems. We can run from small to large lot sizes and also provide custom configurations for OEM orders.



We have X-ray and AOI inspection stations, temperature chambers, plus other test equipment to maintain and verify the quality and manufactureability of the products. All boards are subjected to 100% functional testing. A bar code system tracks each board and lot during the manufacturing process. Using automated electronic assembly methods allows us to increase production and improve response time to our customers while adhering to our high quality standards.

Customer Applications

WinSystems has a diverse customer base which ranges from small companies to Fortune 500 corporations. Our customers depend on us to deliver products and services that help them do their job better and more easily.

- Robotics
- Industrial Automation
- Test Equipment
- Process Control
- Energy Management
- Telecommunications
- Blood Analyzers
- Lab Instruments
- Security Systems
- Data Logging
- Chemical Processing
- Weighing Systems
- Satellite Stations
- Oceanography
- Laser Systems
- Pipeline Control
- Avionics Test
- Microwave Systems
- Weather Stations
- Telescope Controls
- Transportation
- Power Station Monitoring
- Utilities

Call us today. Our goal is to be your embedded product supplier of choice both now and in the future.

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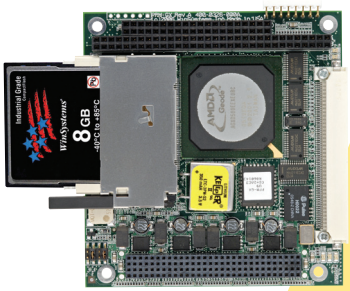
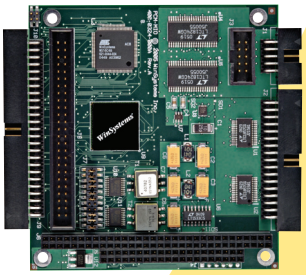
EBX, EPIC and PC/104 SBCs

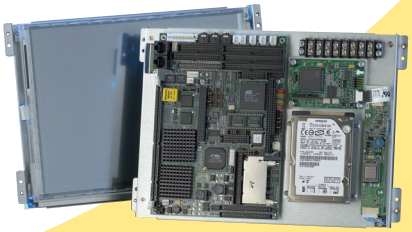


SUMIT-ISM and PC/104 I/O Modules



Enclosures

Panel PCs



Quick Start Kits

Embedded Solutions Catalog