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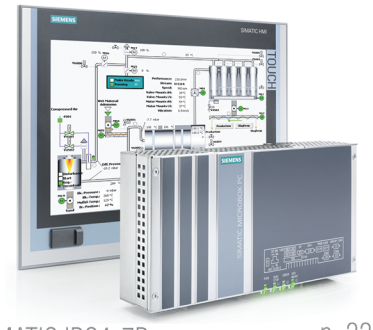

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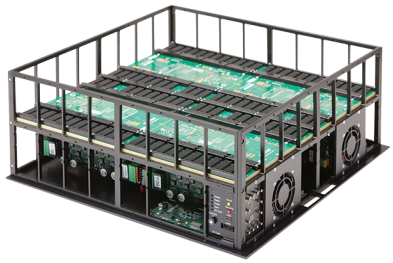

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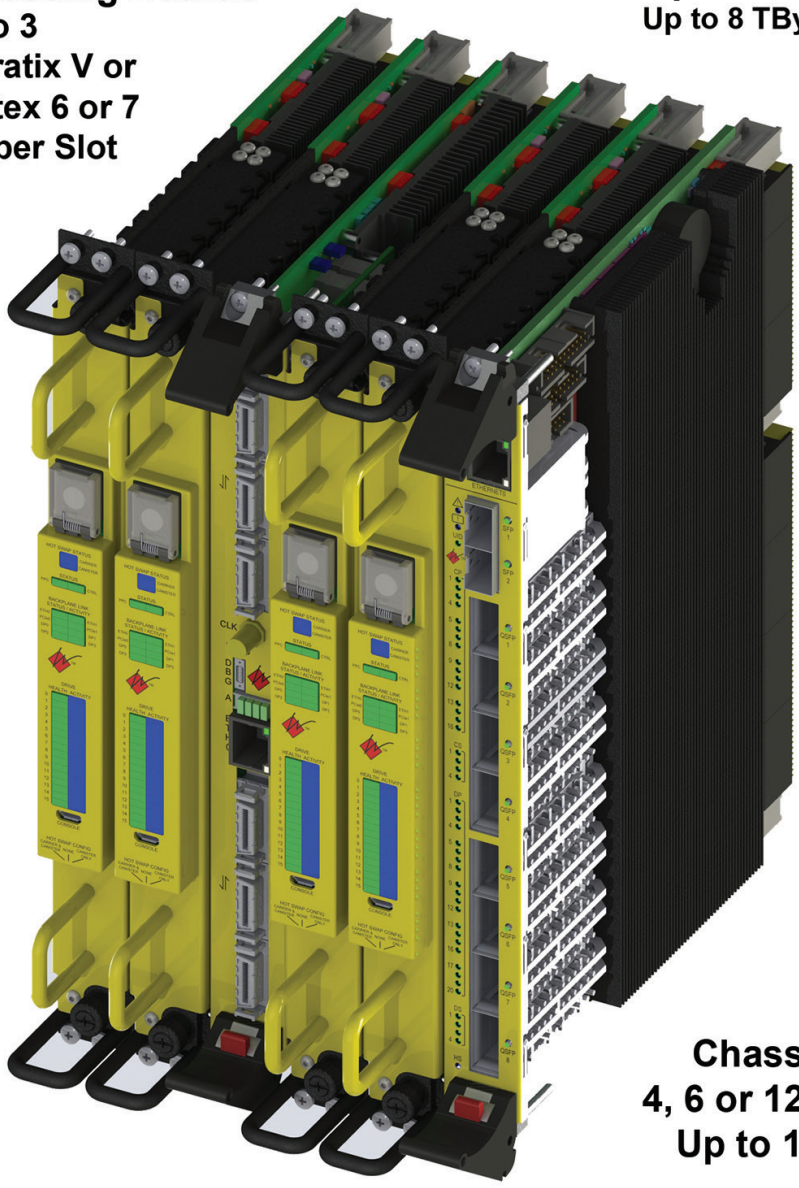

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Annapolis Micro Systems

High Performance Signal and Data Processing in Scalable COTS FPGA Computing Fabric

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By Will Strauss

wis@fwdconcepts.com

Acquisitions and dissolutions shuffle the mobile market deck

Intel's surprise mobile acquisition

Late last month, Intel quietly acquired Tempe, Arizona-based Fujitsu Semiconductor Wireless. To my knowledge, no news announcement has been made, but this is a very important move for Intel as Fujitsu Wireless had developed probably the most advanced multimode LTE RF transceiver available in the open market. The operation traces its lineage through Freescale Semiconductor, the previous owner, and earlier Motorola Semiconductor. Intel has acquired a truly seasoned technical staff, now probably their most experienced U.S.-based wireless talent.

Why no news release? I suspect that Intel was not eager to embarrass its former-Infineon staff in Germany, which has been the major player in 2G/3G RF transceivers and has shipped a multimode LTE RF transceiver (but not an LTE modem) in selected Motorola Droid smartphones.

The new Intel operation's latest RF transceiver product includes advanced features like antenna tuning and envelope tracking. With its internal DSP that also supports smart antennas, device support for any application processor is accommodated (even an x86 … wink, wink). The team has been busy working on the next-gen LTE-Advanced solution preparing for Carrier Aggregation designs.

Renesas Mobile post Nokia-Windows partnership

You may recall that in mid-2010 Renesas Electronics Corporation acquired Nokia's wireless modem operation and added the group to its new subsidiary, Renesas Mobile Corporation. Renesas Electronics had licensed the Nokia modem since 2009 and the two companies had been working together to develop an industry-leading HSPA+/LTE platform.

Unfortunately for Renesas Mobile, Nokia decided to throw its future into the arms of Microsoft's Windows Mobile OS. But the only way Nokia could bring Windows Mobile to market quickly was to employ Qualcomm's readily available modem and application processor platform (Snapdragon). It appears that move cost Renesas Mobile its biggest modem customer. Moreover, Renesas Mobile was never able to find another big customer for its own worthy multimode LTE modem that I mentioned in my last newsletter.

Renesas Electronics tried to sell the Mobile subsidiary, but there are few companies who are big enough to afford absorbing the substantial wireless design staff that would go with such an acquisition. After all, the major smartphone companies already have committed modem chip relationships: Apple, HTC, and Nokia with Qualcomm; Samsung with Samsung Semiconductor; Intel with its own newly minted modem operation, etc. There are probably a dozen Chinese companies who would love to have the Renesas Mobile technology, but most aren't big enough to absorb the Renesas headcount. That leaves licensing of the IP as probably the remaining viable option for Renesas.

The future of the ST-Ericsson split

Now that Ericsson owns the modem properties and STMicroelectronics (STM) owns the application processor product line of the former merged company, I'll make some quick observations:

Ericsson's modem business has reverted to what used to be called the Ericsson Mobile Platforms (EMP) division. EMP was a leading supplier of complete 3G baseband/RF platforms to the handset industry before the ST-Ericsson (STE) merger, rivaling what was then Infineon Technologies.

Ericsson is still shipping standalone TD-SCDMA modems in China (11 percent market share in 2012), GSM/EDGE modems (9 percent share in 2012), and WCDMA/HSPA+ modems (2 percent share in 2012). However, Ericsson now has a very worthy multimode LTE modem and RF transceiver product – the latest "Thor" part of the STE "NovaThor" combined product.

Ericsson's best near-term prospects will be to provide LTE/TD-SCDMA modem/RF transceivers that can appeal to China Mobile's many prospective smartphone suppliers. Those smartphone suppliers can get application processors on their own (or maybe buy them from STM). Better yet, Ericsson should consider adding LTE to the NovaThor 9240 integrated dual-core com-processor approach for China's TD-SCDMA market (licensing IP for the AP from STM?).

STM now retains the "Nova" part of the ambitious STE combined product, namely the ARM-based application processor product line. Although the prospects of getting an STM application processor in a major smartphone are dim (who doesn't already have one?), at least STM can employ the device in other multimedia devices, including the automotive market, where they have better prospects. Or, they can partner with Ericsson for the China Mobile market, mentioned above.

As always, I encourage your feedback.

On the cover

DSPs are becoming more versatile with the combination of ARM processors and increasing number of sensors in IoT devices. And with connected devices, secure FPGAs will become even more important. Find the latest DSP, FPGA, and other products in our 2013-14 Resource Guide.


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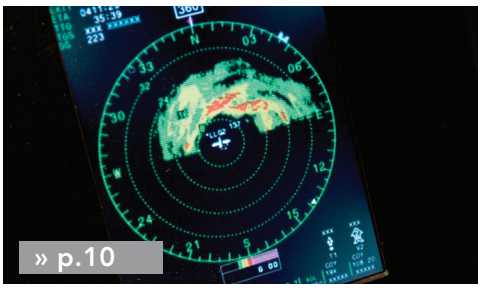
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GUEST COLUMN

By *Mark Littlefield*

mark@luminancetech.com

Year of the FPGA … Maybe?

For years FPGAs have been a workhorse of high-performance embedded DSP. The massively parallel nature of FPGAs is ideal for solving tough problems in the SWaP-limited embedded DSP domain. However, COTS board-level suppliers have struggled to integrate user-programmable FPGA-based products into their product portfolios and to make money from them. High component costs and long development times have meant that such products tend to be both expensive and have a very low return-on-investment for the COTS supplier. As a result, many smaller players remain small, and the larger players who have FPGA-based product lines have not seen the levels of sales or growth that more traditional single-board computers or DSP/multiprocessor boards have previously enjoyed.

Despite this, the benefits of having user-programmable FPGAs as part of a system solution are simply too valuable to pass up. As a result, nearly every COTS board supplier to the embedded community introduced new products with user-programmable FPGAs in the 2012/2013 timeframe. Could it be that COTS-based FPGA's time has finally arrived?

There are a number of factors that are contributing to this seeming explosion of activity. The value of FPGAs to the embedded DSP community continues to skyrocket due to huge jumps in logic cell counts, high-speed serial transceiver rates and channel counts, and specialized embedded processors, DSP slices, and hard-core protocol blocks. In addition, it seems that the FPGA suppliers have finally figured out that they are not designing for and selling to FPGA HDL developers any longer; they are providing tools to make it easier for hardware designers, software developers, and systems engineers to work with FPGAs as part of a larger system.

While there are a number of notable tools improvements from each of the vendors, one standout is Altera's adoption of OpenCL as a fully supported programming model. This introduces the possibility of increasing the pool of available FPGA developers beyond the relatively rare (and expensive) community of VHDL/Verilog HDL developers. It seems that Xilinx has seen the wisdom of this and announced in September their own support for OpenCL-based development as part of their "All Programmable Abstractions" initiative, which itself paints a good picture of where Xilinx wants to go tools-wise.

In addition, the adoption of the ARM architecture and the AMBA AXI bus (Advanced Microcontroller Bus Architecture/Advanced eXtensible Interface) by Xilinx, Altera, and Microsemi is a significant development. It means that the interface wars may finally be over! Developers can now standardize on a single interface specification for their designs, which goes a long way towards promoting reuse and shorter development times. This is long overdue, and very much welcomed by the community.

The net results of these developments are generally positive to both the COTS board supplier and the system integrator. For both it means improved time to market and lower development costs, which is a very strong argument when making design decisions for a new product. For the FPGA suppliers this translates to greater adoption of their products (as witnessed by all of the new products being rolled out).

Not everything is a walk in the park, however. For the board designer the large number of power supplies needed for an FPGA design continue to be a burden. The recent Altera acquisition of Enpirion – who makes very compact power supply components – may indicate a move toward integrating power supply circuits directly on die, much like Intel with their recent Haswell processors.

Many of the new design tools are still in the early days. It may be too soon to declare victory for developments such as AMBA-AXI and OpenCL. Only time will tell whether they are widely adopted and have a real impact on development costs and time to market or deployment (my bet is, they will). Looking forward, these improvements may only be the tip of the iceberg. Issues such as security (information assurance, for example), safety critical design, and design verification and reliability continue to trouble system designers who are looking at FPGA-based solutions. Compared to a common interface and a more friendly development language, these are tough problems that may take years to fully wring out.

Lastly, FPGAs are seeing real competition from new "traditional" DSP processors and the new GPU-based solutions. There are now several COTS GPU boards designed specifically for the high-performance embedded DSP market. Clearly, the FPGA suppliers see this and are positioning their OpenCL support to offset this threat. Though we have yet to see if they are successful.

So, is it the year of the FPGA? Maybe. It's really too soon to tell. However, this is clearly an interesting time for the DSP market.

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DSP-FPGA.com Editorial/Production Staff

Monique DeVoe, Assistant Managing Editor
mdevoe@opensystemsmedia.com

Amanda Harvey, Assistant Editor
aharvey@opensystemsmedia.com

David Diomede, Art Director
ddiomede@opensystemsmedia.com

Mark Littlefiled, Technical Contributor

Sales Group

Tom Varcie
Senior Account Manager
tvarcie@opensystemsmedia.com

Rebecca Barker
Strategic Account Manager
rbarker@opensystemsmedia.com

Eric Henry, Strategic Account Manager
ehenry@opensystemsmedia.com

Ann Jesse, Strategic Account Manager
ajesse@opensystemsmedia.com

Kathleen Wackowski, Strategic Account Manager
kwackowski@opensystemsmedia.com

Susan MacLeod, Strategic Account Manager
smacleod@opensystemsmedia.com

Christine Long
Vice President, Online Business
clong@opensystemsmedia.com

Asia-Pacific Sales
Elvi Lee, Account Manager
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Regional Sales Managers
Barbara Quinlan, Southwest
bquinlan@opensystemsmedia.com

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dseger@opensystemsmedia.com

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sstarr@opensystemsmedia.com

Reprints and PDFs

republish@opensystemsmedia.com

EMEA

Rory Dear
Technical Contributor
rdear@opensystemsmedia.com

Gerry Rhoades-Brown
Account Manager – Europe
gerry.rhoadesbrown@husonmedia.com

Christian Hoelscher
Account Manager – Europe
christian.hoelscher@husonmedia.com

Lauren Palmer
Account Manager – Europe
lauren.palmer@husonmedia.com

OpenSystems Media Editorial/Production Staff

John McHale, Editorial Director
Military Embedded Systems
jmchale@opensystemsmedia.com

Joe Pavlat, Editorial Director
xTCA and CompactPCI Systems
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Brandon Lewis, Associate Editor
xTCA and CompactPCI Systems
PC/104 and Small Form Factors
blewis@opensystemsmedia.com

Lisa Daigle, Assistant Managing Editor
Military Embedded Systems
ldaigle@opensystemsmedia.com

Curt Schwaderer, Technology Editor
Embedded Computing Design

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Corporate

opensystemsmedia.com

Patrick Hopper, Publisher
phopper@opensystemsmedia.com

Karen Layman, Business Manager

30233 Jefferson
St. Clair Shores, MI 48082
Tel: 586-415-6500

Rosemary Kristoff, President
rkristoff@opensystemsmedia.com

Wayne Kristoff, CTO

Emily Verhoeks, Financial Assistant

16626 E. Avenue of the Fountains, Ste. 201
Fountain Hills, AZ 85268
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Subscriptions

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By Steve Edwards

defensesales@curtisswright.com

COTS ADC and DAC converters meet demand for high-performance sense and response applications

For demanding sense and response applications, such as Electronic Attack (EA), Electronic Countermeasures (ECM), and jamming, a key attribute is low latency. For these applications what matters most is how quickly warfighters can identify and respond to a "signal of interest" such as an incoming missile. The closer to real-time a "spoofing" signal can be sent out to fool a foe into thinking the aircraft is where it isn't can make the difference between evading or being destroyed by the threat. To convert the wideband signal spectrum into digital information useful to onboard processing systems requires the fastest, highest-performance Analog-to-Digital (ADC) and Digital-to-Analog (DAC) converters available.

Over the last year or so, various trends have come together that enable COTS vendors to deliver solutions that achieve unprecedented levels of high-bandwidth/low-latency performance. These trends include the use of open standards designed for deployed rugged military environments and higher levels of bandwidth and resolution available from ADC and DAC products leveraged from commercial markets, such as the high-end test equipment market. Today's compute-intensive sense and response applications require very high ADC performance that combines wide bandwidth, low latency, and Spurious Free Dynamic Range (SFDR). Defense and aerospace system designers now have access to a new generation of ADC products from leading vendors such as Texas Instruments and Analog Devices that deliver 12+ bit resolution and bandwidth rated at >4 Gsps.

Today, the best performing ADC/DAC devices are found in the test and measurement world. This is because the oscilloscopes and other tools used to measure the performance of cutting edge electronics systems need to be significantly faster than the system being tested. In partnership with Curtiss-Wright, Tektronix Component Solutions, a manufacturer of ADC/DAC devices used in the commercial test and measurement market, is now bringing their electronic components to the COTS defense and aerospace market. For Electronic Warfare (EW) applications, the benefit is straightforward: The 12.5 Giga-Sample Per Second (GSps) data rates and up to 9 GHz of instantaneous bandwidth delivered by Tektronix's Silicon Germanium (SiGe)-based devices provide coverage for a larger slice of the RF spectrum due to their wider bandwidth.

Effective sense and response solutions need not only high data rate and low latency ADCs and DACs, they also need the processing infrastructure to implement the necessary DSP, data paths, and fast memory buffers to match. The good news is that the latest generation of FPGAs, such as Xilinx's Virtex-7, are well-matched to this task – they can support fast, wide data interfaces and provide several hundred thousand to over one million logic cells, and 3,600 DSP slices which provide nearly a TFLOP of DSP processing, as well as SERDES that can operate at 10.3 Gbaud over a VPX backplane. The result is the data flow can be routed through a single device, which is the optimum architecture for low latency processing.

By bringing these data conversion and FPGA processing components together on rugged platforms for harsh airborne and ground vehicle platforms, COTS vendors are able to offer solutions ranging from multi-TFLOP capable 6U OpenVPX modules to compact/lightweight small form factor 3U modules. Open architecture COTS sense and response processing modules available today include both monolithic solutions and board sets that employ FPGA Mezzanine Card (FMC) modules. FMCs directly connect the I/O devices to the host FPGA. They have no onboard processors, bus interfaces, or bridges, such as PCI, but directly link the physical I/O devices on the FMC to the FPGA on the host board.

An example of a COTS board that brings all of these emerging trends together is Curtiss-Wright's CHAMP-WB (Wideband) signal processing boards. When combined with the TADF-4300 add-on module, jointly designed with Tektronix, the resulting variant is the CHAMP-WB-DRFM (Digital Radio Frequency Memory) 6U OpenVPX board with a Virtex-7 FPGA. Combined, these two modules form the CHAMP-WB-DRFM and deliver 12.5 GSps 8-bit ADC and 12.5 GSps 10-bit DAC performance from a single 6U slot. Future variants of the board will be able to operate in DAC-only mode to deliver full 25 GSps. This board set delivers 3x the performance of any earlier signal processing module and enables airborne warfighters to "see" a wider segment of the wideband signal spectrum (the "horizon") in near real-time while still maintaining good resolution (or "focus"). By combining the CHAMP-WB-DRFM with another CHAMP-WB populated with a pair of 16-bit multi-channel ADC/DAC FMCs, the resulting system can mix both high sampling/moderate resolution (>10 Gsps, 8-10 bits) with lower sampling/high resolution (<1 Gsps, 14-16 bits) in a very low latency system that provides both wideband and narrowband EA capability.

ARM + DSP makes an optimized SoC

By Monique DeVoe, Assistant Managing Editor

The use of ARM CPUs is growing in Systems-on-Chip (SoC) platforms, as the generic ARM architecture lends well to a wide variety of systems and applications. However, while ARM processors are ideally suited for system management functions, they typically struggle with processing-intensive tasks such as imaging and advanced audio and voice communications. As the need for advanced signal processing continues to increase, application-specific Digital Signal Processors (DSPs) are now being integrated with ARM cores on the die of SoCs to offload demanding data processing from the CPU in order to optimize power consumption and performance.

"ARM CPUs are widely used today in a variety of applications, such as mobile computing, home entertainment, wireless communications, and network infrastructure," says Eyal Bergman, VP of Product Marketing, CEVA. "However, the ARM cores cannot handle demanding data processing tasks in a power efficient manner. For that purpose, the ARM cores are augmented with dedicated engines such as advanced vector DSPs to offload the ARM from tasks such as Layer 1 (L1) data processing in cellular communications, and multimedia processing in mobile computing devices. The application-specific DSP is typically integrated alongside an ARM processor, providing 10x more horsepower to deal with [the] latest communication and multimedia requirements while significantly reducing power consumption."

The ARM and DSP combination on SoCs also helps with scalability in addition to performance optimization.

"It is a universally accepted fact that one Instruction Set Architecture (ISA) will not be able to optimally satisfy increases in data processing and changes in scalability requirements," says Sanjay Bhal, Focused End Equipment Manager, HPC and Cloud, Texas Instruments. "With the integration of ARM and DSP in the SoC, customers can now take advantage of the best single threaded performance of an ARM core to run control code while using a DSP core for processing-intensive applications."

Heterogeneous combination challenges

Although heterogeneous processor architectures provide significant benefits in terms of performance and efficiency, integrating ARM cores and DSPs on the same die presents a number of challenges. Developers must now align these heterogeneous architectures with dedicated hardware acceleration blocks and system peripherals, which creates integration and management problems, Bergman says.

"ARM offers industry-standard interconnect IPs [through the] Advanced Microcontroller Bus Architecture (AMBA) protocol to allow multiple heterogeneous cores to be applied on SoC devices in a transparent manner," he says. "In addition, different system IPs are required, such as L1, L2, and L3 caches with full cache coherency, data traffic management IPs, hardware acceleration IPs, and more.

"As an ARM partner, CEVA supports ARM's latest interconnect technologies with its range of DSPs to enable joint CEVA and ARM customers to integrate ARM CPUs with CEVA DSPs seamlessly. In addition, CEVA also offers many proprietary system IPs, such as Direct Memory Access (DMA) and data traffic management using advanced queues and buffers."

The complex hardware of multicore SoCs also leads to software complexity. To simplify software development on these

complex SoCs, programmers need to abstract the different cores and hardware blocks and need to have drivers and APIs to control the blocks, Bhal says.

"Multicore SoC complexity directly translates to software complexity, and while multicore software architecture partitioning, task scheduling, dispatching, and coordination among cores add another layer of programming challenges, they do not have to be overwhelming," says Bhal. "Figuring out how to accelerate multicore software development and still deliver a robust and top-quality system solution are the utmost concerns for multicore developers. Our KeyStone multicore SoCs offload many software functions into hardware AccelerationPacs or other architectural elements in order to reduce the amount of software needed, and to automate many of the more complex multicore management tasks."

Application-specific SoCs and the future

SoCs with integrated application-specific processors are a forward-looking trend as the demands for higher-performance data processing grow. SoCs optimized to deal with the unique requirements of communication, imaging and vision, audio, and voice market segments will provide strong areas of growth for heterogeneous architectures that include DSPs and superscalar ARM cores.

"With the growing desire by cellular subscribers to be 'always on' and the increasing availability of higher bandwidth, we see a constantly growing need for higher performance with more advanced communication technologies such as LTE-Advanced and Wi-Fi 802.11ac; improved imaging and scene analysis such as in Natural User Interface (NUI), higher resolution video, and Advanced Driver Assistance Systems (ADAS); and advanced audio and voice applications such as voice triggering and activation, and HD audio processing for home and automotive," Bergman says. "This trend heavily promotes the need for application-specific processors that can efficiently offload the main system CPU with dedicated optimized support for data processing in the application domain." DSP-FPGA.com

Floating-point multiprocessing with C66x DSPs from Texas Instruments

By Paul Moakes

Fixed-point DSPs store and manipulate integers, while floating-point DSPs use a mantissa and exponent to represent rational numbers. Multiple factors determine whether fixed- or floating-point is the right choice for a particular application, including cost, development time, and performance.

Fixed-point DSPs have tended to be lower priced, while floating-point DSPs have been easier for development while also providing higher accuracy and precision. This means that fixed-point DSPs have been used as high-volume, general-purpose processors, while floating-point DSPs have been chosen for specialized, processing-intensive tasks where dynamic range and precision are important.

Up to now it was often necessary to implement algorithms on fixed-point DSPs because floating-point DSPs were not fast enough, but porting algorithms created with MATLAB or other floating-point tools was slow and time consuming. Texas Instruments Incorporated (TI) changed the game with processors based on its TMS320C66x core, which is capable of both fixed- and floating-point arithmetic.

According to TI, having a DSP core that integrates both fixed- and floating-point capability enables a fundamental change in the way algorithms for embedded systems are developed and deployed.

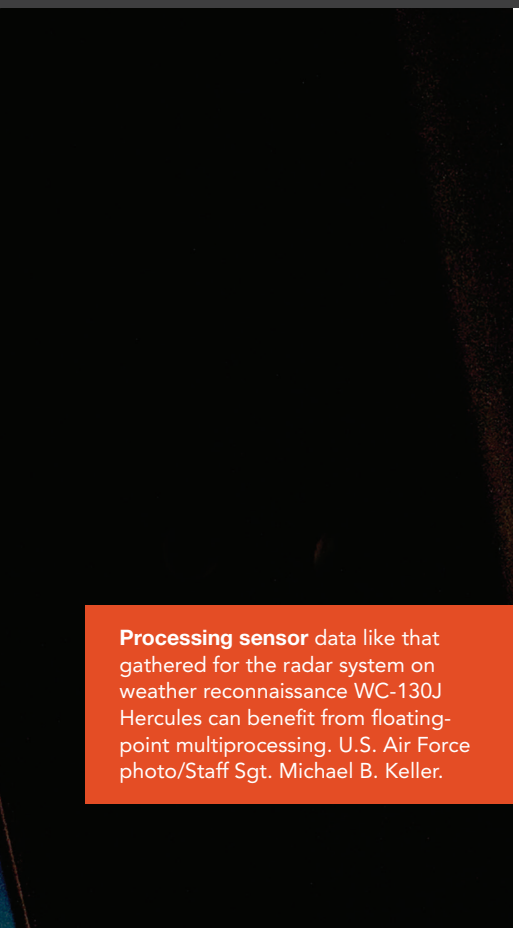
The C66x DSP core provides floating-point capabilities without sacrificing the speed of fixed-point. It achieved this by merging the C67x floating-point and the C64x fixed-point instruction sets into its C66x instruction set. The instruction set architecture is fully IEEE 754 compliant and supports both single- and double-precision floating-point operations. Software can choose to execute floating-point or fixed-point commands on an instruction-by-instruction basis, which enables developers to optimize their code for the needs of their particular application.

Applications for floating-point DSPs

There are many applications with algorithms that can be accelerated by floating-point DSPs and benefit from their improved precision. The increased affordability of DSPs based on the C66x core means that these benefits are more widely available, and retain the capability of fast fixed-point processing for computation that does not require floating-point arithmetic.

For example, in wireless and radio systems, MIMO and beam-forming algorithms rely on matrix inversion techniques inherently susceptible to quantization and scaling errors associated with fixed-point processing. Using floating-point DSPs to implement these algorithms improves both the speed and the accuracy of the system, resulting in higher performance. The C66x DSP core runs MIMO and other key multi-antenna signal processing algorithms four times faster than the same algorithms running in fixed-point on the C64x DSP.

Radar, navigation, and guidance systems process data that is acquired using arrays of sensors. To extract information on the location and movement of the target, the data must be processed as a set of linear equations. With a floating-point engine like the C66x, a greater precision of output can be achieved, as well as a larger dynamic range. A 32-bit fixed-point DSP has a dynamic range of 0 to 4.3×10^{9} with integer resolution. A 32-bit floating-point DSP has a range of 1.2×10^{-38} to 3.4×10^{38}, which means that these functions are performed significantly better than with fixed-point DSPs.



Processing sensor data like that gathered for the radar system on weather reconnaissance WC-130J Hercules can benefit from floating-point multiprocessing. U.S. Air Force photo/Staff Sgt. Michael B. Keller.

Another application that benefits from the accuracy of floating-point is image processing. For example, in ultrasound, the greater precision given by the C66x enables imaging systems to achieve a much higher level of definition and faster recognition due to lower quantization noise, thus improving the diagnostic process.

The new TI DSPs – a closer look

TI offers multiple processors, based on its KeyStone architecture, that incorporate its C66x core. Let's take a closer look at two examples.

First, the TMS320C6678 is based on TI's KeyStone I architecture and includes eight C66x cores each running at up to 1.25 GHz, enabling the equivalent of up to 10 G cycles per second of DSP processing. Executing eight instructions per cycle (and having two-way single-instruction multiple data instruction supports) allows the headline figure of 160 G Floating-point Operations Per Second (GFLOPS) by the device. The C66x core is fully backward compatible with the C6000 family of fixed- and floating-point DSPs.

The TMS320C6678 also provides a comprehensive set of I/O. This includes four lanes of low-latency Serial RapidIO (SRIO) 2.1 at 5 Gbaud per lane full duplex and two lanes of PCIe Gen2, similarly at 5 Gbaud per lane full duplex. An Ethernet MAC subsystem, two telecom serial ports, UART and I2C interfaces complete the conventional interfaces required by today's embedded devices.

In addition to the conventional I/O, the C6678 has a HyperLink interface. This low pin count, point-to-point communication interface is designed to extend internal chip transactions between two KeyStone devices. Supporting high speeds of up to 12.5 Gbaud per lane over four lanes, it can be used to aggregate the device resources of two C6678s DSPs, which can be viewed as a single 16-core system capable of 640 GFLOPS.

The SmartReflex technology of TI's KeyStone devices can also decrease the dynamic power consumption while maintaining performance. Using a dedicated voltage regulator for each device, the device's core voltage is optimized based on the process corner of the device.

Second, the 66AK2H12 processor based on TI's second generation KeyStone architecture (KeyStone II) combines quad ARM Cortex-A15 MPCore processors with eight TMS320C66x DSP cores. With core clocks raised to 1.4 GHz, the 66AK2H12 provides up to 5.6 GHz of ARM and 11.2 GHz of DSP processing power. Its security, packet processing, and Ethernet switching engines make the device a much more powerful wireless embedded processor than ARM Cortex-A15 devices designed for consumer products.

The ARM Cortex-A15 MPCore processor combines leading processing capabilities with a very low power and performance ratio, multicore hardware-based cache coherency, and broad industry software support. By integrating the ARM processors, there is no need in most applications for an additional high-end, general-purpose processor, which greatly reduces system cost and design complexity.

With wide industry adoption of the ARM processors, developers can quickly and easily migrate existing software to the new KeyStone II-based devices. Full ARM-based Linux systems can be created, while offloading real-time processing to the high-performance C66x cores.

For more complex systems that need additional processing capacity, the 66AK2H12 has two HyperLink ports. These can be used to connect multiple KeyStone devices and thus add more C66x DSP cores, more ARM Cortex-A15 processors, or both. HyperLink allows the devices to work in tandem transparently with tasks executed as if running on local devices.

The 66K2H12 is well suited to many applications that need high DSP performance and the control features of the ARM cores, such as high-quality video processing.

Harnessing the power of the C66x DSP core

Let's take the example of the CommAgility AMC-V7-2C6678, a high-performance signal processing AMC card with two 1.25 GHz TMS320C6678 DSPs – giving a total of 16 C66x cores. The two DSPs are linked with HyperLink, providing a connection at up to 50 Gbaud. They can access up to two GB x 64 DDR3-1333 SDRAM each.

Flexible, high bandwidth off-board communications are provided by Gen2 SRIO at up to 20 Gbps per port. As standard, the board provides a single front panel SFP+ optical interface that links directly to the on-board Xilinx Virtex-7 FPGA, plus a mini-SAS connector linked to the SRIO switch. Should applications require timing and synchronization, this is achieved via the front panel or backplane clock I/O.

The card is well suited to a range of high-performance DSP/FPGA processing applications, including telecoms infrastructure and image processing. By providing a high-performance FPGA, large shared memory and fast, flexible I/O, the horsepower of the TI DSPs can be harnessed and used effectively, while keeping power consumption, physical size, and cost within tight limits.

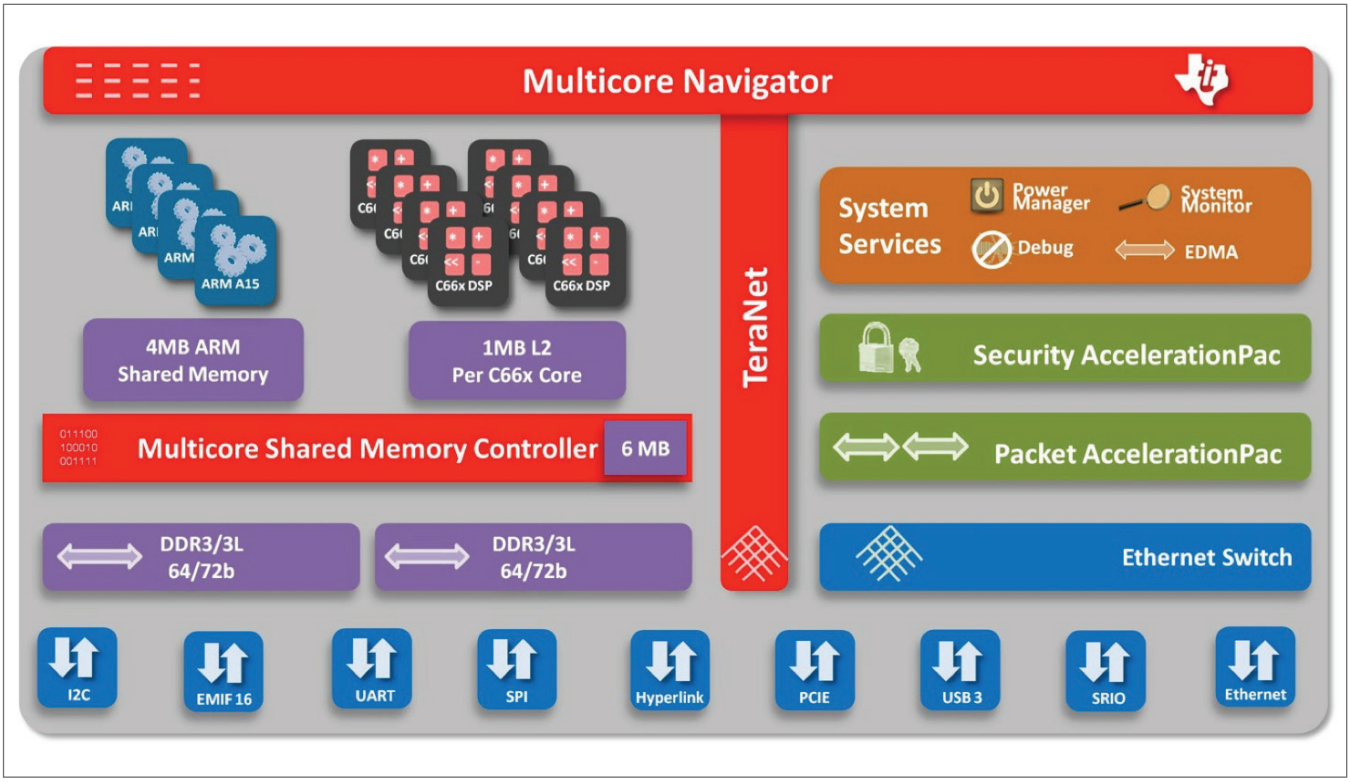


Figure 1 | 66AK2H12 System-on-Chip (SoC). (Image courtesy of Texas Instruments)

Application example: machine vision

As the demand for higher resolutions and new algorithms is rising in machine vision, a big increase in processing performance is needed. In one example, the CommAgility AMC-2C6678L was chosen as the main processing board, with the board's two C66x DSPs undertaking sorting and analyzing tasks.

Previously, all processing in the application used fixed-point arithmetic. The C66x DSPs' integration of floating-point and fixed-point capabilities now makes it easier to quickly undertake test implementations of new algorithms, or to use algorithms that need a high dynamic range of input and output data.

Also, TI now supports the OpenMP and OpenCL specifications on the KeyStone family. This helps in distributing the load on the various cores when using algorithms that can be easily parallelized. These technologies are useful for rapid implementations, but in the long term it can be more effective to distribute the workload across the cores using different tasks in the DSPs' SYS/BIOS real-time kernel, and with the hardware facilities provided by TI's Multicore Navigator. DSP-FPGA.com

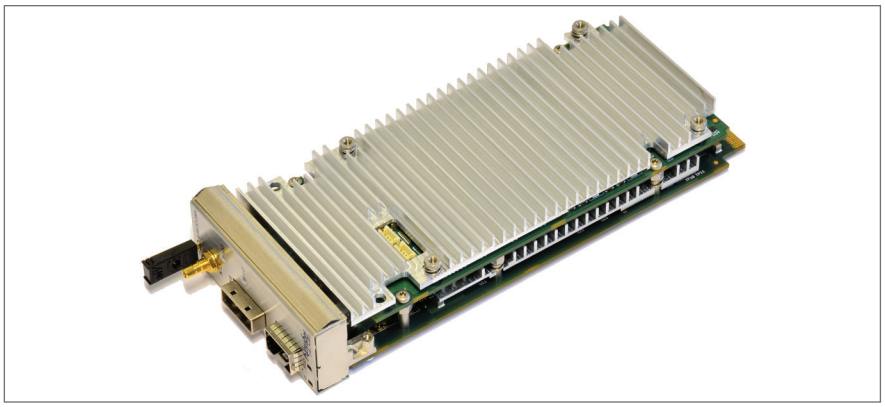


Figure 2 | CommAgility AMC-V7-2C6678.

For more information on Texas Instruments DSPs, see: www.ti.com/lsds/ti/dsp/overview.page

Paul Moakes *Ph.D. MIET is Technical Director at CommAgility. He has previously been employed by Motorola, Blue Wave Systems, and Marconi Instruments. He holds two patents in the field of MicroTCA and AdvancedMC. He received his Ph.D. in Electrical and Electronic Engineering from Sheffield University, and a First Class Honours degree in Electronic Communications and Computer Systems Engineering from Bradford University.*

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paul.moakes@commagility.com
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ARM Cortex-M4-based microcontrollers bring energy efficiency and high performance to intelligent applications

By Rasmus Larsen

Many designers are on a quest to embed intelligence into even the most mundane objects as they try to equip smart homes with intelligent connected devices and sensor networks that link to the burgeoning Internet of Things (IoT). Other embedded designers focus on increasing the capabilities of already-intelligent consumer electronics products or on making portable versions of sophisticated sensing devices that require energy efficiency. Though these intelligent devices often need to run on battery power for a long time – sometimes for a period of years – many also require high performance due to their complexity.

Power efficiency

Today's Microcontroller (MCU) market is abuzz with talk about ultra-low energy consumption measured in Nanoamps (nA). All of these power-sensitive embedded applications need MCUs that will function reliably. This trend has culminated in the recent launch of the ARM M0+ processor, a stripped-down, ultra-low-power processor core intended for just these applications.

However, MCUs based on the more powerful ARM Cortex-M4 processor with an integrated Floating Point Unit (FPU) are also being used. This core offers more performance, including floating-point and DSP instructions. Most MCU vendors position their M4-based products as high-performance solutions supported by complex software libraries, assuming that truly energy-sensitive applications will require a stripped-down processor.

So why would anyone choose a low-energy MCU equipped with FPU and DSP functions? The first reason is that, perhaps counter intuitively, such a processor may in fact prove to be more energy efficient than a less powerful device. The availability of floating-point and single-cycle multiply-accumulate instructions often allows the designer to reduce execution time, or reduce the clock frequency to accomplish the same workload. Put simply, expending 10 percent more power for 20 percent less time represents an energy saving overall.

This effect is accentuated in devices with well-designed sleep modes that deliver very low power. For instance, the Silicon Labs Wonder Gecko MCU has five distinct low-energy modes, including a 20 nA shut-off state and 950 nA deep sleep mode (running real-time clock, full RAM and register contents retained and brown-out detector enabled). The bigger the difference between active and sleep mode power consumption, the greater the benefit will be of a rapid return to a low-energy state.

Ultrasonic water metering is one example of such a use case that, in addition to signal processing, also requires outstanding sleep mode performance, as well as battery life measured in years. In such an application, an ARM Cortex-M4 based MCU can be

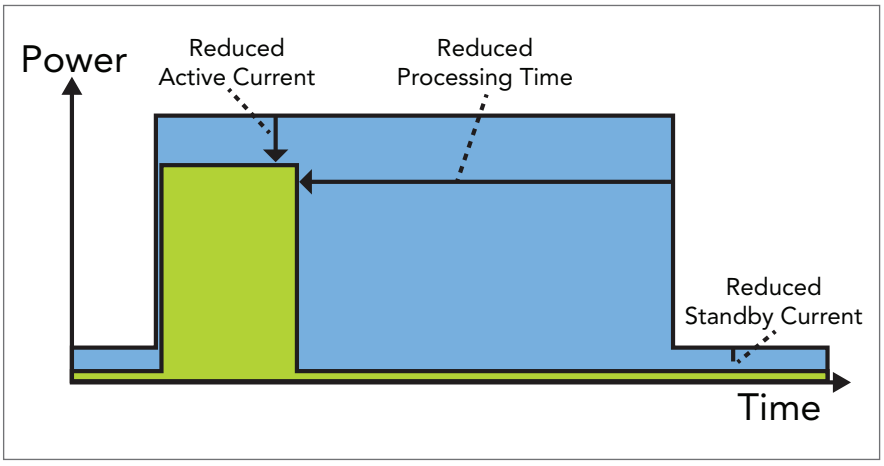

Figure 1 | The saved energy (blue area) increases when an application is optimized by increasing the processing speed and reducing the active and sleep current.

configured with the CPU in sleep mode and its peripherals set up as a kind of analog state machine that wakes the Cortex-M4 processor only when water is flowing. The availability of DSP instructions allows the designer to build sophisticated filtering functions that come into action when there is water flow to measure, eliminating the need for expensive ultrasonic transducers.

High performance

Some applications simply need the processing horsepower of a DSP. Consider, for example, a security device that senses glass breakages using acoustic analysis. The sensors rely on both audio and shock, or vibration, of shattered glass to determine if someone is breaking in.

For such sensors to reliably report break-ins and not be triggered when keys fall to the floor, the telephone rings, or even when a drinking glass breaks, the sensor logic needs to perform numerous complex operations. To positively detect and confirm a window breaking, the sensor also needs to analyze pre-break actions: was there an impact or flexing of the glass prior to shattering? Secondly, the sensor needs to consider the shattering frequencies, the audio of breaking glass, within a defined time frame. After filtering the frequency information, the duration and amplitude of the signal are checked to provide further verification of a valid alarm condition.

Low power without sacrificing performance

The MCU used in a glass break detector performs fast Fourier transforms on the output from a wideband sound transducer to determine whether a breakage has taken place. The use of a DSP-enabled MCU allows glass break analysis to be performed much faster than software-based solutions. And with a sensor interface that only wakes up the processor when actual glass-break frequencies are detected, the total energy consumption can be reduced as well. This in turn enables sensors to become wireless and battery operated, making them more tamper-proof and easier to install and retrofit into existing security systems.

Because the glass break detection system needs to run for a period of years from a single battery, it must be designed so that the MCU wakes up and starts processing only when a possible acoustic event has occurred. The chip's fast wake-up capabilities facilitate this energy efficiency, and its DSP capabilities minimize wake time while allowing the system designer to choose a detection algorithm that is robust against false alarms.

Portable medical equipment provides another typical example of a power-sensitive application that requires long battery life without sacrificing performance. Battery-powered ECGs are becoming increasingly popular portable medical devices, but the fact is, to obtain a really accurate read-out of cardiac health, the patient often needs to visit a hospital or health clinic for a comprehensive ECG. The processing power of many current portable devices, including ECGs, is restricted by the power and energy budget imposed by battery-based operation. As a result, designers compromise system performance by reducing sampling rates. DSP-equipped low-energy processors present a practical solution to this design challenge by enabling higher system performance without significantly reducing battery life.

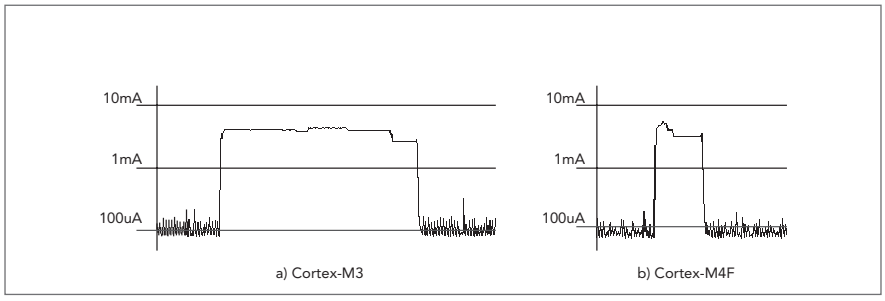

Figure 2 | Applications save energy when staying in sleep energy modes while FPU- and DSP-enabled MCUs solve tasks faster. A 512-point FFT is 3x more energy efficient on the Cortex-M4 to the right.

Achieving the right balance, for the right price

Power-sensitive applications like glass break detectors and portable medical devices demonstrate that low-energy operation is not always about paring processing power to the bone. Tomorrow's energy-efficient products require high-performance, FPU-capable MCUs offering the right balance of processing capabilities, low active power consumption, well-designed sleep modes, and optimized, autonomous mixed-signal peripherals.

Such considerations also come into play in the field of smart sensing and the IoT. As MCU prices have dipped below the dollar mark, it has become increasingly possible to put intelligence into everyday objects. A DSP-equipped MCU provides a special type of intelligence that can be used for signal conditioning purposes. By siting such processors at the location where each signal is captured, designers can choose lower cost sensor types, increasing the range of applications that can cost-effectively be addressed.

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Rasmus Christian *Larsen, Applications Engineering Manager, Microcontroller Products, heads Silicon Labs applications engineering teams for EFM32, EFR and Ember ZigBee solutions. Based in Oslo, Norway, he joined Silicon Labs in July 2013 with that company's acquisition of Energy Micro, the leading supplier of energy-friendly ARM based solutions. As one of the designers of Energy Micro's first microcontroller series, the EFM32 Gecko, Rasmus has in-depth knowledge of the complete EFM32 product family. He previously worked as a digital design engineer for Atmel AVR and has a master's degree in electronics from The Norwegian University of Science and Technology (NTNU) in Trondheim, Norway.*

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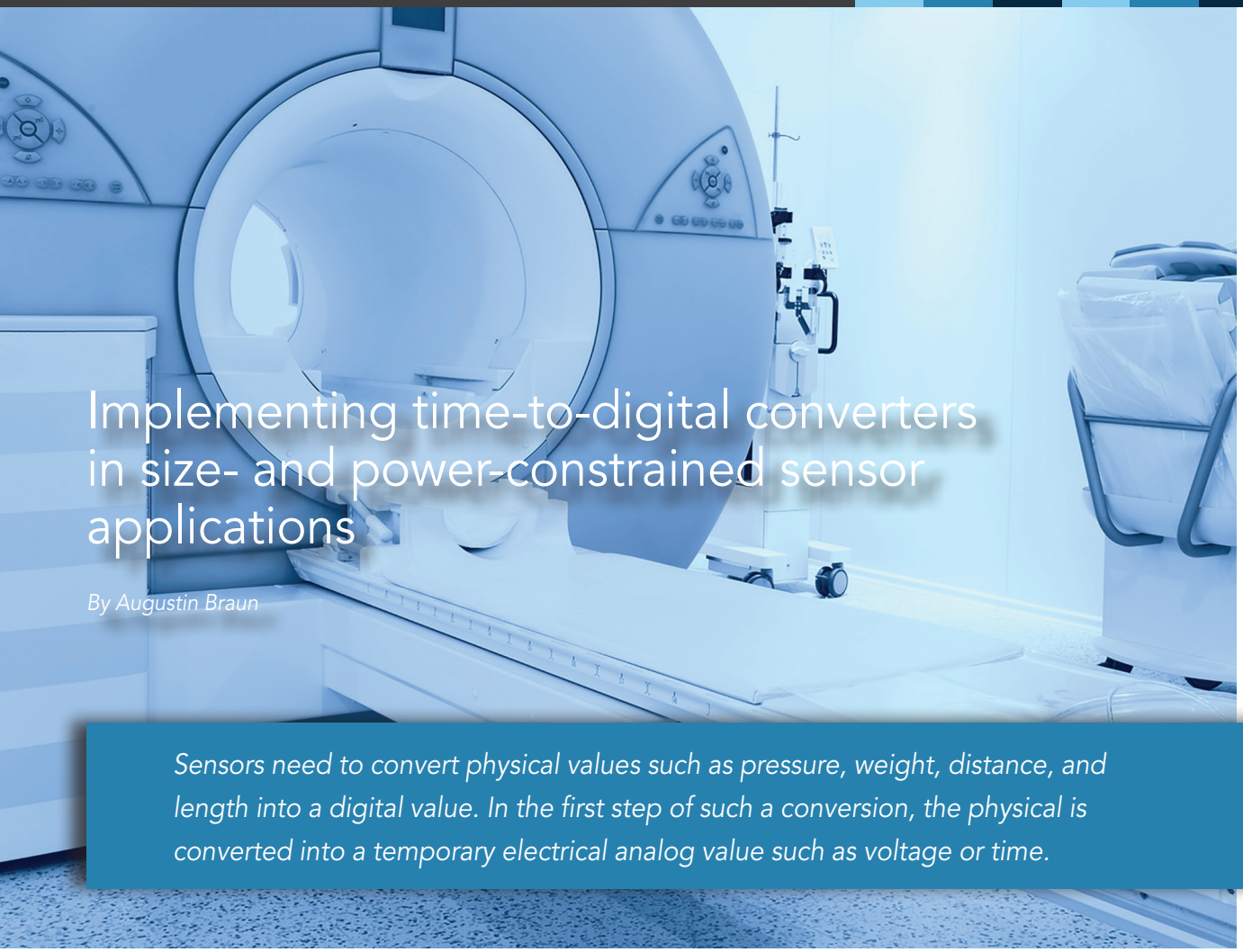

Implementing time-to-digital converters in size- and power-constrained sensor applications

By Augustin Braun

Sensors need to convert physical values such as pressure, weight, distance, and length into a digital value. In the first step of such a conversion, the physical is converted into a temporary electrical analog value such as voltage or time.

Analog-to-Digital Converters (ADC), which currently dominate in market presence, use electrical voltage as a temporary value. For example, a weight is converted with a Wheatstone bridge and strain gages into a differential voltage. An ADC converts the differential voltage to a digital value.

A Time-to-Digital Converter (TDC) can do the same type of analog-to-digital operation, but the difference with TDCs is that time is used as a temporary value ("time") instead of volt-age. With a Resistor-Capacitor (RC) circuit, a weight is converted with strain gages into a time difference. A TDC converts the time difference to a digital value. The basic principle is the same. Only the temporary value during the process of conversion is different.

Though historically ADCs have been primarily used, TDCs can offer technical advantages in size, ease of development, and power consumption.

Process technology challenges alleviated

TDCs are undemanding in matters of process technologies. A TDC is basically a purely digital circuit. No special process technologies in the wafer fabrication are required for them to become more powerful. Everything can be integrated and manufactured on standard CMOS processes.

Today's sensor applications often require intelligent front-end systems. Such digital intelligence (such as microprocessors and non-volatile memory) must operate with the converters in the smallest spaces. A TDC is capable of being manufactured in all kinds of wafer process technologies. The integration of a high-resolution ADC into a System-on-Chip (SoC) can be challenging and can potentially cause problems at migration to smaller process technologies such as at the deep-submicron level, and at migration to altered wafer process technologies. With a standard microprocessor today, for example, a 10 bit to 12 bit ADC is integrated. However, even at a 14-bit resolution, measurements are very imprecise. High-end ADCs can achieve 24-bit resolution, which is a 4,000 times higher resolution when used in standard microprocessors.

In contrast, a TDC is easy to migrate from one technology to another because of its digital nature, and automatically improves performance at smaller process technologies due to taking up less die space, which facilitates faster gate switching and less switching delay. A migration requires minimal R&D effort with little risk of failure due to a TDC's ease of porting digital values. A TDC in general can achieve a resolution of 30 bits because time can be measured and resolved much more precisely than analog voltage. Such resolution is achieved regardless of having an on-chip microprocessor or not. TDCs are undemanding because they are built with digital gates that are the same as the ones in a microprocessor.

Simplified front-end design
TDCs also require little effort for front-end design. In contrast, an ADC needs a very good pre-amplifier with a stable and precise amplification of 50 to 200 times to measure strain gages. Such a pre-amplifier is more difficult to develop and port to a different process technology.

A TDC needs an analog front-end circuit for the conversion into time; however, in most cases the required circuits are very simple and easy to integrate on different wafer process technologies. For the same set-up as the ADC example above, a TDC does not need a pre-amplifier. The sensor signals can be compared directly with simple comparators. The reason for this is the inherently higher 30-bit resolution of a TDC. All the problems caused by pre-amplifiers and portability do not exist with TDCs.

Low power consumption
More and more battery-powered applications drive the demand for less and less power consumption. With a TDC, such power-optimized applications can be realized without modification. TDCs are quickly and easily turned on and off; the power-consuming circuit for signal processing at high-precision measurements can be switched on only when it is really needed.

For example, designers are facing battery-powered applications that require a 10-year life cycle in permanent operation. As such, little power is available to run the system. Ultrasonic heat meters with a TDC-based IC inside are capable of processing everything from temperature and ultrasonic measurements within as little as 2 µA power consumption. This gives enough room for the power needed to operate the microprocessor and covers the remaining tasks needed in applications such as heat meters. The requirements of an ultrasonic water meter are between 5 and 10 times higher.

Case study: Ultrasonic flow metering
To achieve an ultrasonic flow measurement with the required accuracy, the time difference must be resolved into the lower picosecond (ps) range, such as 50 ps (Figure 1). With a "normal" counter, developers would need a clock frequency of 20 GHz for this task; that cannot be achieved without a lot of time and effort.

Acam uses the gate delay of digital circuits (such as those from an inverter) to resolve in the picosecond range. It measures how many gate delays have passed in a certain time difference. Acam developed digital circuits to measure almost any time difference stable over temperature, voltage changes, and process variations. Also, for increased resolution requirements, these TDCs address the complete spectrum of measurement applications. They have a stable resolution starting at 10 ps (TDC-GPX), and 98 percent of all available applications can be covered with that. The high resolution demanded today is no longer an obstacle. Easily a resolution below 5 ps can be achieved and covers demand. Converter integration in a complex product on a deep-submicron process can lead to a smart solution with very little silicon area consumption.

The future of TDCs
Demands for integrating TDCs will rise as do the demands for smaller ICs, higher integration, more integrated intelligence, smart sensors, little or almost no power consumption, faster product development, and flexibility to quickly generate new products in alternative process technologies. Semiconductor manufacturers have yet to invest and promote TDC technology as a parallel technology to ADCs, but niche applications are utilizing TDC circuits and have come to dominate metering segments with big market shares. TDCs already cover more than 90 percent of the ultrasonic flow metering market share, more than 70 percent of magnetostrictive ultrasonic position-ing, more than 50 percent of positron emission tomographs for cancer diagnosis tools, and double digit percentages of industrial and science segments.

Additionally, new sensor segments continue to adopt TDC technology. In the field of capacitive sensor elements, TDCs fit almost perfectly to measurement requirements. Capacitive MEMS sensors and complex sensor systems need powerful converters and built-in intelligence to cover the sensors of the future. TDCs can address the challenges in these applications, and embedded developers will recognize their advantages to the demanding applications of the future.

Augustin Braun, *together with Andreas Larsch, is CEO and owner of acam messelectronic gmbh, a company located in Stutensee near Karlsruhe, Germany, that is specialized in solutions and concepts for highly precise measurement technology.*

acam messelectronic gmbh
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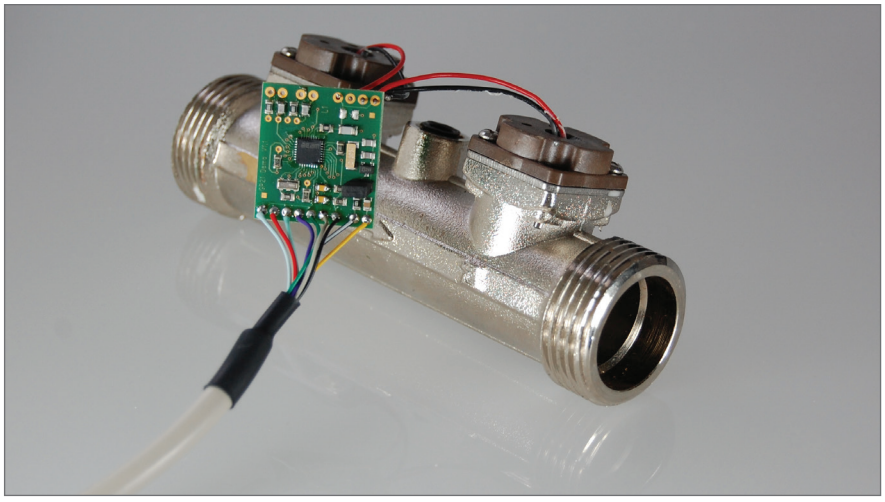

Figure 1 | Ultrasonic water and heat metering with acam TDC-GP22.

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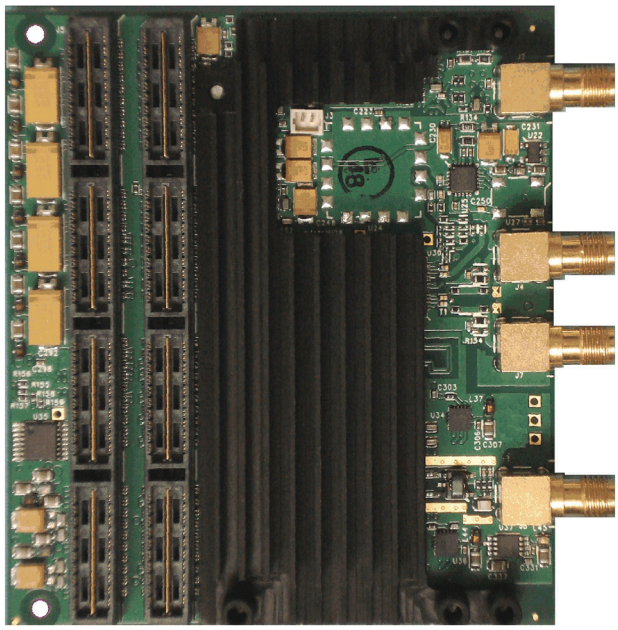

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The **Annapolis Micro Systems Dual Channel 4.0 GSps D/A I/O Card** provides one or two 12-bit digital output streams at up to 4.0 GSps. The board has one or two MAX 19693 for 4.0 GSps, MAX 19692 for 2.3 GSps, or MAX 5859 for 1.5 GSps.

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In concert with the WILDSTAR 4 or WILDSTAR 5 FPGA processing main boards, this mezzanine board supplies user-configurable real-time A to D conversion and digital output. Up to two A/D or D/A and up to two serial I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VME/VXS or IBM Blade main board, or up to one A/D or D/A and up to one serial I/O card on each PCI-X or PCI Express main board.

Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. VHDL source is provided for the interfaces to A/Ds, D/As, DRAM/SRAM, LAD bus, I/O bus, and PPC Flash. CoreFire™ users will have the usual CoreFire Board Support Package.

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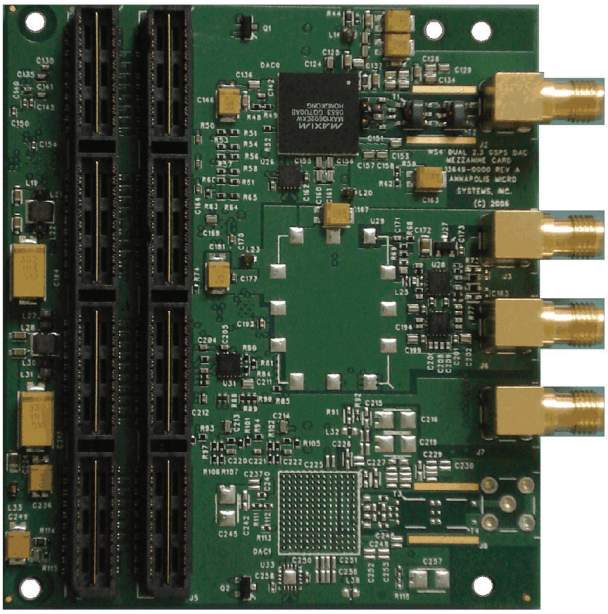

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- Five SMA front panel connectors: two single-ended DAC outputs, one high-precision trigger input with Fs precision
- One universal single- or double-ended 50 ohm clock input
- High-precision trigger input manufacturing options – 1.65 V LVPECL, 2.5 V LVPECL, 3.3 V LVPECL
- I/O card plugs onto WILDSTAR 4 or 5 VME/VXS/PCI-X/PCI Express/ IBM Blade main boards
- JTAG, ChipScope, and Serial Port access
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for board-level interfaces
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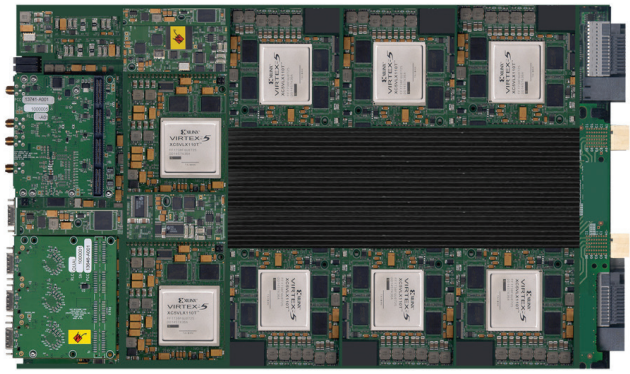
Annapolis Micro Systems, Inc. is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, Digital Signal Processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores. Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. A graphical user interface for design entry supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules.

WILDSTAR 5 for IBM Blade, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Achieve world-class performance; WILDSTAR solutions outperform the competition.



FEATURES

- From two to eight Virtex-5 FPGA processing elements – LX110T, LX220T, LX330T, FX100T, FX130T, or FX200T; six are pluggable with power module and memory
- Up to 10.7 GB DDR2 DRAM per WILDSTAR 5 for IBM Blade Board
- 144 x 144 crossbar; 3.2 Gb per line; two external PPC 440s – 1 per each I/O FPGA
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Available in both commercial and industrial temperature grades
- Proactive thermal management system – board-level current measurement and FPGA temperature monitor, accessible through host API
- Includes one-year hardware warranty, software updates, and customer support
- Blade management controller; USB, RS-485, Ethernet, KVM, 16 RIO, Switch to 1 GbE over backplane
- Save time and effort; reduce risk with COTS boards and software
- We offer training and exceptional special application development support, as well as more conventional support
- Famous for the high quality of our products and our unparalleled dedication to ensuring that the customer's applications succeed

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WILDSTAR 6 for OpenVPX

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. Our 14th-generation WILDSTAR 6 for OpenVPX uses Xilinx's newest Virtex-6 FPGAs for state-of-the-art performance. It accepts one or two I/O mezzanine cards in one VPX slot or up to four in a double wide VPX slot, including Single 1.5 GHz 8 Bit ADC, Quad 250 MHz 12 Bit ADC, Single 2.5 GHz 8 Bit ADC, Quad 130 MHz 16 Bit ADC, Dual 2.3/1.5 GSps 12 Bit DAC, Quad 600 MSps 16 Bit DAC, Universal 3Gbit Serial I/O (Rocket I/O, 10 Gb Ethernet, InfiniBand), and Tri XFP (OC 192, 10G Fibre Channel, 10 Gb Ethernet). Our boards work on a number of operating systems, including Windows, Linux, Solaris, IRIX, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

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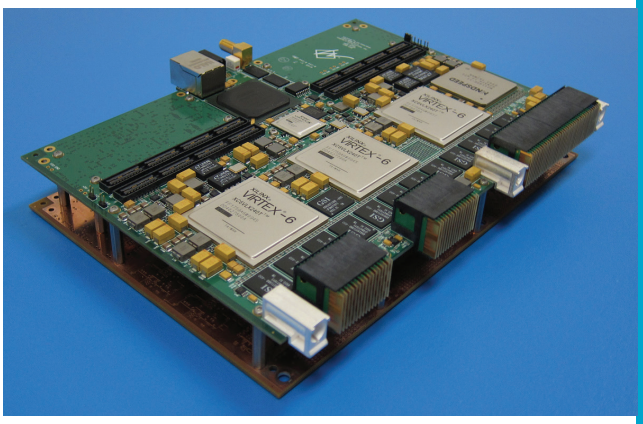

FEATURES

- Up to three Virtex-6 FPGA processing elements – XC6LX240T, XC6LX365T, XC6LX550T, XC6SX315, or XC6SX475
- Up to 7 GB DDR2 DRAM in 14 banks or up to 448 MB DDRII or QDRII SRAM
- OpenVPX backplane
- 80 x 80 crossbar connecting FPGAs and VPX backplane
- 1 GHz 460EX PowerPC onboard host
- 4X PCIe controller
- Programmable Flash to store FPGA images and for PCI controller
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope Access
- Host software: Windows, Linux, VxWorks, etc.
- Available in both commercial and industrial temperature grades
- Proactive Thermal Management System – Board level current measurement and FPGA temperature monitor, accessible through host API
- Save time and effort and reduce risk with COTS boards and software; achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

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SIEMENS

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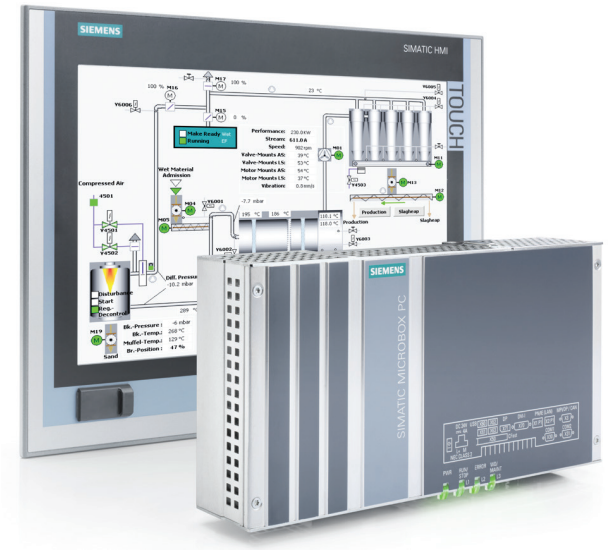
SIMATIC IPC 427D/477D

The **SIMATIC IPC 427D/477D** Industrial PCs are both equipped with 0the latest 3rd generation Intel i7 processors and offer the highest performance – without a fan. With these computers you can implement complex, demanding and maintenance-free automation solutions, such as measuring, operating, controlling, handling, or monitoring. Both form factors, box and panel IPC, rely on the same hardware platform. This reduces your evaluation effort because common drivers, uniform engineering, and simple single parts management can be used. Moreover, training efforts for employees are reduced. The common platform is also equipped with the latest hardware features, such as USB 3.0, Display Port, and CFast, a fast, externally accessible mass storage. In addition, due to support by the Intel Core i7 processors, SIMATIC IPCs can use Intel AMT which allows remote controlling and remote maintenance of IPCs.

The Microbox 427D is highly efficient and highly flexible, even in ambient temperatures of up to 55 °C. The box PC can be configured with one or two additional PCI-e extension slots, Profinet or Profibus onboard. The panel PC 477D is available as touch or touch/key version, with display sizes ranging from 12-22". All panel computers are equipped with industrial-suited, widescreen front panels which rely on the established Siemens front concept. They feature brilliant imaging, due to high resolution and a high viewing angle; high energy efficiency, due to LED backlighting that is 100% dimmable; maximum ruggedness, due to fronts made of die-cast aluminum.



FEATURES

- **High performance, fanless:** Maximum performance in an embedded device
  - Intel Core-i7 processor (3rd gen.) with Turbo Boost
  - HD graphics with dyn. frequency integrated in the processor
  - 8 GB DDR3 RAM and ECC support
  - Fast, rugged bulk memories (SSD 160 GB, CFast 16 GB)
  - State-of-the-art interfaces (USB 3.0, DisplayPort)
  - Fanless operation up to ambient temperatures of 55 °C
- **Flexibility and expandability:** Seamless system upgrades and expansion
  - Up to two PCIe expansion slots
  - Numerous interfaces onboard (4 x high-speed USB 3.0, COM, 2 x Gigabit Ethernet)
  - Multi-monitoring with DVI and DisplayPort interface for two monitors
- **Ruggedness, minimal maintenance:** 24-hour continuous operation without maintenance
  - No rotating parts (fan, HDD)
  - Battery-free – (also applies to retentive memory option)
  - High temperature, vibration, shock and EMC resistance
  - Fanless operation up to ambient temperatures of 55 °C
- **Easy integration:** Easy integration thanks to maximum application flexibility
  - Flexible installation positions with DIN rail, wall and portrait assembly (diagnostics LEDs always visible)
  - Interfaces on one side for easy wiring
  - Remote operation and maintenance via Intel AMT
  - Numerous certifications and approvals, e.g. shipbuilding, CE, UL, FM Class 1 DIV 2
- **Rapid commissioning:** Unpack, Connect, Go!
  - Pre-installed and activated 32- or 64-bit Windows operating system
  - Turnkey bundles with pre-installed control software WinAC RTX (F) as well as pre-installed visualization software
  - WinCC Advanced/Professional (in preparation)

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Innovative Integration
a subsidiary of Interconnect Systems, Inc.
... real time solutions!

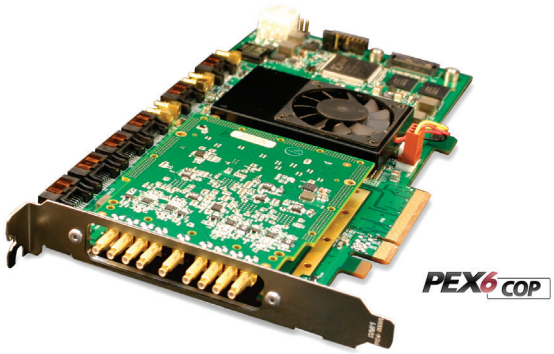
www.innovative-dsp.com/products.php?product=PEX6-COP

PEX6-COP PCI Express Desktop/Server

The **PEX6-COP** is a flexible FPGA coprocessor card that integrates a Virtex-6 FPGA computing core with an industry-standard FMC I/O module on a half-length PCI Express desktop or server card.

The FPGA computing core features the Xilinx Virtex-6 FPGA family, in densities up to LX550 and SX475. An FMC site, conforming to VITA 57, provides configurable I/O for the PEX6-COP.

Download data sheets and pricing now!



FEATURES

- Desktop/Server Half-length FPGA coprocessor card
- FMC I/O site (VITA 57) with x10 5 Gbps MGT lanes, 80 LVDS pairs (LA, HA, HB full support)
- FPGA Computing Core
- Xilinx Virtex-6 SX315T, SX475T, LX240T or LX550T
- 2 Banks of 1GB DRAM (2GB total)
- 2 banks of 9MB QDRII+ SRAM (18MB total)
- 128MB DDR3 DRAM, 32Mb flash
- Dual sample clock input

Innovative Integration | 805-578-4260

Contact: sales@innovative-dsp.com

Innovative Integration
a subsidiary of Interconnect Systems, Inc.
... real time solutions!

http://innovative-dsp.com/products.php?product=FMC-310

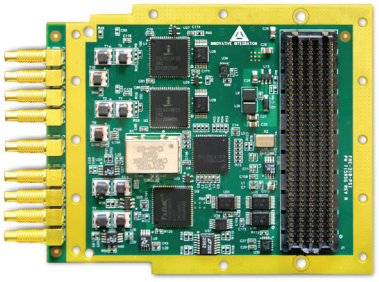
FMC-310

The **FMC-310** is a high speed digitizing and signal generation FMC I/O module featuring four 310 MSPS A/D channels supported by sample clock and triggering features.

Analog I/O may be either AC or DC coupled. Receiver IF frequencies of up to 155 MHz are supported. The sample clock is from either an ultra-low-jitter PLL or external input. Multiple cards can be synchronized for sampling.

The FMC-310 power consumption is 6W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

Support logic in VHDL is provided for integration with FPGA carrier cards. Specific support for Innovative carrier cards includes integration with Framework Logic tools that support VHDL/Verilog and Matlab developers. The Matlab BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator for the FMC integrated with the FPGA carrier card.



FEATURES

- Four A/D Inputs
  - 310 MSPS, 16-bit
  - AC or DC coupled
- Sample clocks and timing and controls
  - External clock/reference input
  - Programmable PLL
  - 10 MHz, 0.5 ppm reference
  - Integrated with FMC triggers
- FMC module, VITA 57.1
  - High Pin Count no SERDES required
  - Compatible with 1.2 to 3.3V VADJ
  - Power monitor and controls
- 6W typical (AC-coupled inputs)
- Conduction Cooling per VITA 20 subset
- Environmental ratings for -40° to 85°C 9g RMS sine, 0.1g^2/Hz random vibration

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Contact: sales@innovative-dsp.com

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WILD OpenVPX Four Slot Mesh Chassis

Annapolis enters the OpenVPX market with **WILDSTAR 6 Xilinx Virtex-6** and **WILDSTAR A5 Altera Stratix 5 FPGA Processing Boards**, an 8 TB per slot WILD Storage Solution, a WILD Switch, a Four Slot and a Twelve Slot Chassis.

The **Four Slot Mesh Chassis** has a particularly powerful Backplane Configuration, as shown in the diagram.

The chassis could, for example, be filled with two of the 8 TB WILD Storage Cards, one WILDSTAR A5 Stratix V FPGA Processing Board, and a Single Board Computer.

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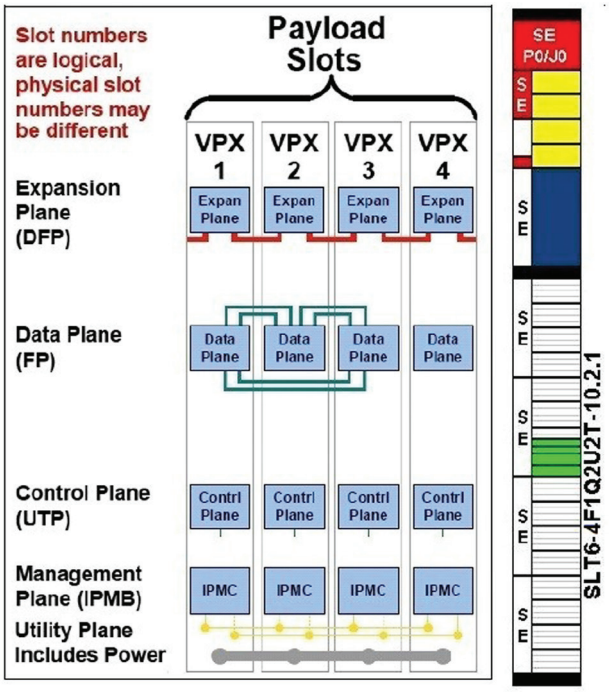

FEATURES

- 4U High 19" Rack Mount Chassis with Front Mounted Horizontal OpenVPX Card Cage with Four Slots
- 4 Slot OpenVPX High Speed Mesh Backplane with Rear Transition Module Support
- 10+GBps on Data Plane for 10GBase-KR Ethernet, 40GBase-KR4 Ethernet, 10GBase-KX4 XAUI or SDR, DDR and QDR 4x InfiniBand
- 8x PCIe Gen 1, 2 or 3 on Expansion Plane
- 1000Base-X on Control Plane
- Large Power Supply
- Chassis Management, including Voltage, Temperature and Fan Monitoring and Control and a Front of Chassis Display Panel
- High Performance Convection Cooling with Replaceable and Cleanable Fan Tray and Filter
- Front Panel Power Switch, System Rest Switch and Maskable Reset Switch, all with Safety Covers
- Electromagnetic Shielding
- Includes one year hardware warranty

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

Save time and effort and reduce risk with COTS boards and software. Achieve world-class performance – WILD solutions outperform the competition.

Annapolis Micro Systems, Inc. | 410-841-2514

Contact: wfinfo@annapmicro.com

Annapolis Micro Systems

www.annapmicro.com

WILD OpenVPX Storage Board

Annapolis leads the **OpenVPX** market with the 8 Terabyte per slot WILD Storage Solution with 4GBps Write and 8GBps Read Bandwidth. The **Storage Board** has a Hot Swappable Canister containing up to 16 Pluggable 1.8" SSD SATA 3.x Drives, with 2, 4 or 8 Terabytes per Board.

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FEATURES

- 4 GBps Write and 8 GBps Read Bandwidth
- Up to 40Gb Ethernet or QDR InfiniBand on each of Four Fat Pipes on P1 for a total of 20GBps on P1
- PCI Express 8x Gen 1, Gen 2 or Gen 3 on P2 and P5 of the OpenVPX Backplane
- 2, 4 or 8 Terabytes per OpenVPX Slot
- Hot Swappable Canister
- Up to 16 Pluggable 1.8" SSD SATA 3.x
- API for Command and Control of the Storage Process
- Includes one year hardware warranty

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WILD OpenVPX Switch Board

Annapolis leads the OpenVPX market with the **WILD 6U OpenVPX** (VITA 65.0 Compliant) **Switch Board**, with up to 4 Tbps non-blocking switching capacity with up to 8 switch partitions.

Supports OpenVPX Switch Profiles: SLT6-SWH-20U19F-12.4.1: 20 Control Plane and 19 Data Plane Backplane Ports; SLT6-SWH 16U20F-12.4.2: 16 Control Plane and 20 Data Plane Backplane Ports; SLT6-SWH-24F-12.4.3: = 24 Data Plane Backplane Ports.

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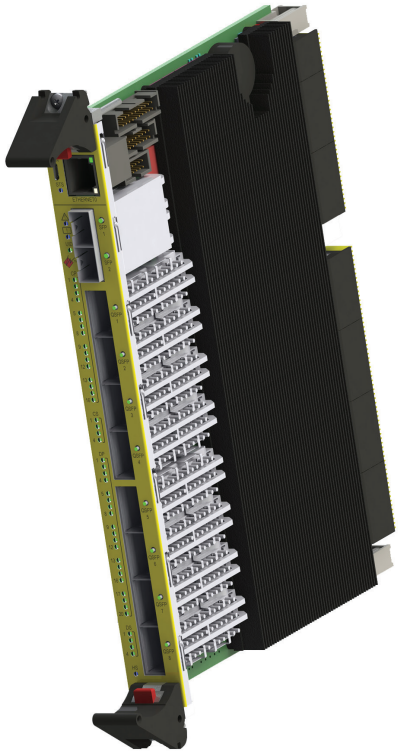

FEATURES

- 6U OpenVPX Board
- Up to 4Tbps Non-Blocking Switching Capacity with up to 8 Switch Partitions
- Multiprotocol Switch – SDR/DDR/QDR/FDR InfiniBand and 1/10/20/40 Gb Ethernet
- Each Backplane and Front Panel Port can be Configured for either InfiniBand or Ethernet
- Front Panel: Up to 8 QSFP+, Up to 2 SFP+, RJ45 Management Port, USB USART, LED Status
- Supports OpenVPX Switch Profiles
- InfiniBand and IP Routing
- Ethernet Gateways
- ChMc Management Plane Support
- Includes one year hardware warranty

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WILD OpenVPX Twelve Plus 3 Slot Switched Chassis

Annapolis enters the OpenVPX market with WILDSTAR 6 Xilinx Virtex-6 and WILDSTAR A5 Altera Stratix 5 FPGA Processing Boards, an 8 TB per slot WILD Storage Solution, a WILD Switch, a Four Slot and a Twelve Plus Three Slot Chassis.

With Ten Payload Slots and Two Switch Slots, and an option for Three VME/VPX Slots, the **Twelve OpenVPX Plus 3 Chassis** has a particularly powerful Backplane Configuration, as shown in the diagram.

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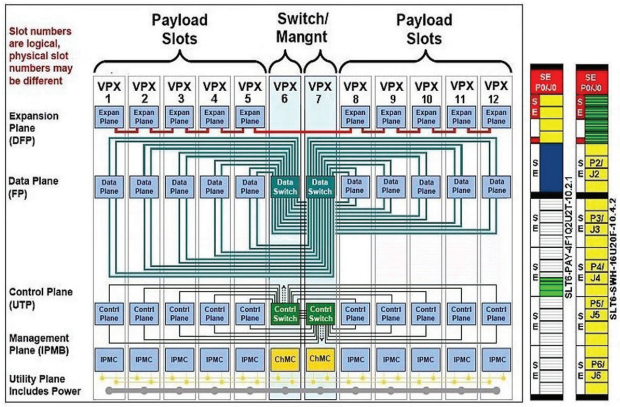

BKP6-CEN12-11.2.XXX

FEATURES

- 19" Rack Mount Chassis with Front Mounted OpenVPX Card Cage
- Primary Twelve Slot 6U OpenVPX High Speed Switched Backplane with Rear Transition Module Support
- 10+GBps on Data Plane for 10GBase-KR Ethernet, 40GBase-KR4 Ethernet, 10GBase-KX4 XAUI or SDR, DDR and QDR 4x InfiniBand
- 8x PCIe Gen 1, 2 or 3 on Expansion Plane
- 1000Base-X on Control Plane
- Secondary Three Slot VME/VPX Backplane for Power Only Payload Cards
- Very Large Power Supply
- Chassis Management, including Voltage, Temperature and Fan Monitoring and Control and a Front of Chassis Display Panel
- High Performance Convection Cooling with Replaceable and Cleanable Fan Tray and Filter
- Front Panel Power Switch, System Rest Switch and Maskable Reset Switch, all with Safety Covers
- Electromagnetic Shielding
- Includes one year hardware warranty

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WILDSTAR A5 for OpenVPX

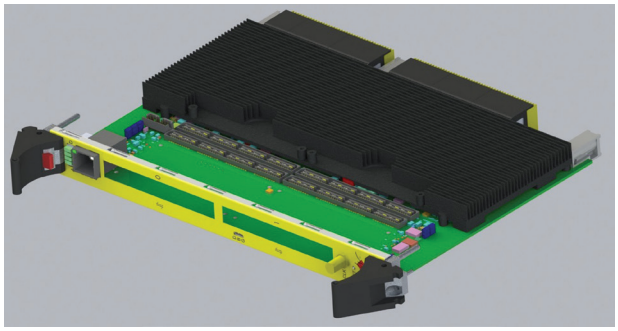
Supports up to Twenty-four 14G InfiniBand, Six 40Gb Ethernet, or Twenty-four 10G Ethernet Connections.

WILDSTAR A5 for OpenVPX uses Altera's newest Stratix V FPGAs for state-of-the-art performance. This is one of a series of Altera Based FPGA Processing Boards from Annapolis.

Annapolis Micro Systems, Inc. is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. It accepts up to four I/O mezzanine cards, including Single 1.5 GHz 8 Bit ADC, Quad 250 MHz 12 Bit ADC, Single 2.5 GHz 8 Bit ADC, Quad 130 MHz 16 Bit ADC, Dual 2.3/1.5 GSps 12 Bit DAC, Quad 600 MSps 16 Bit DAC, Universal 3Gbit Serial I/O (RocketIO, 10 Gb Ethernet, InfiniBand), and Tri XFP (OC 192, 10G Fibre Channel, 10 Gb Ethernet). Our boards work on a number of operating systems, including Windows and Linux. We support our board products with a standardized set of drivers, APIs and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR A5 for OpenVPX, with its associated I/O Cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.



FEATURES

- Supports up to Twenty-four 14G InfiniBand, Six 40Gb Ethernet, or Twenty-four 10G Ethernet Connections
- Up to Three Altera Stratix V FPGA Processing Elements – GSD4, GSD5, GSD6, GSD8, GXA3, GXA4, GXA5, GXA7, GXA9, GXAB
- Up to 8 GBytes DDR3 DRAM in 4 Memory Banks and Up to 80 MBytes QDRII + SRAM in 5 Memory Banks per WILDSTAR A5 for OpenVPX Board
- Programmable FLASH for each FPGA to Store FPGA Images
- APM86290 PowerPC on Board Host
- PCI Express Bus Gen 1, Gen 2, or Gen 3 to P2 Expansion Plane through On Board PCIe Switch
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope Access
- Available in both commercial and industrial temperature grades
- Proactive Thermal Management System – Board Level current measurement and FPGA temperature monitor, accessible through Host API
- Includes one year hardware warranty, software updates, and customer support
- Training available

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

Save time and effort and reduce risk with COTS boards and software. Achieve world-class performance – WILD solutions outperform the competition.

Annapolis Micro Systems, Inc. | 410-841-2514

Contact: wfinfo@annapmicro.com

Annapolis Micro Systems

www.annapmicro.com

WILDSTAR A5 for PCI Express

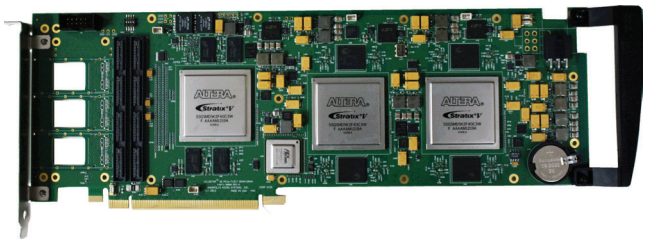
Supports up to Three 56G FDR InfiniBand, Three 40Gb Ethernet, or Twelve 10Gb Ethernet Connections.

WILDSTAR A5 for PCI Express uses Altera's newest Stratix V FPGAs for state-of-the-art performance. This is the first of a series of Altera Based FPGA Processing Boards from Annapolis.

Annapolis Micro Systems, Inc. is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. It accepts one or two I/O mezzanine cards, including Single 1.5 GHz 8 Bit ADC, Quad 250 MHz 12 Bit ADC, Single 2.5 GHz 8 Bit ADC, Quad 130 MHz 16 Bit ADC, Dual 2.3/1.5 GSps 12 Bit DAC, Quad 600 MSps 16 Bit DAC, Universal 3Gbit Serial I/O (RocketIO, 10 Gb Ethernet, InfiniBand), and Tri XFP (OC 192, 10G Fibre Channel, 10 Gb Ethernet). Our boards work on a number of operating systems, including Windows and Linux. We support our board products with a standardized set of drivers, APIs and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR A5 for PCI Express, with its associated I/O Cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.



FEATURES

- Supports up to Three 56G FDR InfiniBand, Three 40Gb Ethernet, or Twelve 10Gb Ethernet Connections
- Up to Three Altera Stratix V FPGA Processing Elements – GSD4, GSD5, GSD6, GSD8, GXA3, GXA4, GXA5, GXA7, GXA9, GXAB
- Up to 4 GBytes DDR3 DRAM in 2 Memory Banks and Up to 192 MBytes QDRII + SRAM in 12 Memory Banks per WILDSTAR A5 for PCI Express Board
- Programmable FLASH for each FPGA to Store FPGA Images
- 16X PCI Express Bus Gen 1, Gen 2, or Gen 3 to Host PC through On Board PCIe Switch
- Supports PCI Express Standard External Power Connector
- Multi Channel High Speed DMA
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope Access
- Available in both commercial and industrial temperature grades
- Proactive Thermal Management System – Board Level current measurement and FPGA temperature monitor, accessible through Host API
- Includes one year hardware warranty, software updates, and customer support
- Training available

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

Save time and effort and reduce risk with COTS boards and software. Achieve world-class performance – WILD solutions outperform the competition.

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WILDSTAR 6 for AMCs

Annapolis Micro Systems, Inc. is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications. Our fourteenth generation WILDSTAR 6 for AMC uses Xilinx's newest Virtex-6 FPGAs for state-of-the-art performance. It accepts one FMC I/O Card. Our boards work on a number of operating systems, including Windows, Linux, Solaris, IRIX, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and also provides proven, reusable, high-performance IP modules. WILDSTAR 6 for AMC, with its associated I/O Cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

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Save time and effort and reduce risk with our COTS boards and software. Achieve world-class performance – WILD solutions outperform the competition.

FEATURES

- One Xilinx Virtex-6 FPGA I/O Processing Elements – LX240T, LX365T, LX550T, SX315T or SX475T
- On board Host Freescale P1020 or P2020 PowerPC
- Up to 2.5 GBytes DDR2 DRAM in 5 memory banks or
- Up to 80 MB DDRII or QDRII DRAM in 5 memory banks
- Programmable FLASH to store FPGA image
- 4X PCI Express Bus Gen 2 between PPC and FPGA
- Supports VITA 57 FMC I/O Cards
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Available in both commercial and industrial temperature grades
- Proactive Thermal Management System – current, voltage, and temperature monitoring sensors via Host API
- Includes one year hardware warranty, software updates, and customer support. Training available.

Annapolis Micro Systems, Inc. | 480-841-2514

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WILDSTAR 6 PCIe

Annapolis Micro Systems, Inc. is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications. Our fifteenth-generation **WILDSTAR 6 for PCI Express** uses Xilinx's newest Virtex-6 FPGAs for state-of-the-art performance. It accepts one or two I/O mezzanine cards, including Single 1.5 GHz 8 Bit ADC, Quad 250 MHz 12 Bit ADC, Single 2.5 GHz 8 Bit ADC, Quad 130 MHz 16 Bit ADC, Dual 2.3/1.5 GSps 12 Bit DAC, Quad 600 MSps 16 Bit DAC, Universal 3Gbit Serial I/O (RocketIO, 10 Gb Ethernet, InfiniBand), and Tri XFP (OC 192, 10G Fibre Channel, 10 Gb Ethernet). Our boards work on a number of operating systems, including Windows, Linux, Solaris, IRIX, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

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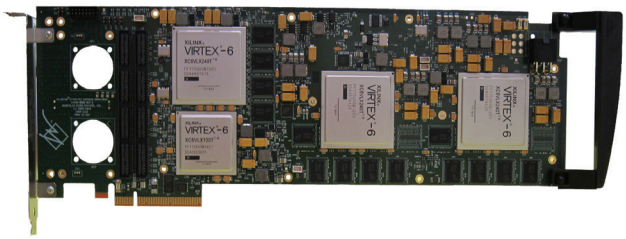

FEATURES

- Up to three Xilinx Virtex-6 FPGA I/O processing elements – LX240T, LX365T, LX550T, SX315T, or SX475T
- Up to 8 GBytes DDR2 DRAM or DDR3 DRAM in 14 memory banks per WILDSTAR 6 for PCI Express board or up to 480 MBytes DDRII+/QDRII DRAM in 15 memory banks
- Programmable FLASH for each FPGA to store FPGA images
- 8X PCI Express Bus Gen 1 or Gen 2
- Supports PCI Express standard external power connector
- High-speed DMA Multi-Channel PCI controller
- Full CoreFire Board Support Package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Available in both commercial and industrial temperature grades
- Proactive Thermal Management System – Board Level current measurement and FPGA temperature monitor, accessible through Host API
- Includes one year hardware warranty, software updates, and customer support. Training available.

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Mini-K7

The **Mini-K7** is a user-customizable, turnkey embedded instrument that includes a full Windows/Linux PC and supports a wide assortment of ultimate-performance FMC modules. With its modular I/O, scalable performance, and easy to use PC architecture, the Mini-K7 reduces time-to-market while providing the performance you need.

Distributed Data Acquisition – Put the Mini-K7 at the data source and reduce system errors and complexity. Optional GPS or IEEE1588-synchronized timing, triggering and sample control is available for remote I/O. Limitless expansion via multiple nodes. Up to 4 SSD for data logging.
Uniquely customizable – dual FMC sites for IO, user-programmable FPGA for IO interfaces, triggering and timing control, USB ports.
Remote or Local Operation – Continuous data streaming up to 3200 MB/s to SSD or Gb/s Ethernet. Optional, stand- alone, autonomous operation with GPS-synchronized sampling.
Rugged – SSD boot drive support in a compact, rugged footprint that is ready for embedded operation
8-26V DC-Only Operation – Perfect for portable or automotive data loggers or waveform generators.

FEATURES

- Combines an industry-standard COM Express CPU module with a single FMC I/O module in an extremely compact, stand alone design
- Programmable Kintex 7 325/410 and Spartan 6 FPGAs
- Small form factor: 4" H x 7" W x 10" D
- Conduction cooled design: Fins or cold-plate
- Dual VITA 57 FMC IO module site. Add anything from RF receivers to industrial control modules
- I/O site (VITA 42.3) delivers >3000MB/s to CPU memory
- Integrated timing and triggering support for IO includes GPS, IEEE1588 or IRIG -disciplined clock
- Supports Innovative and third-party FMC modules for private data channels, triggering and timing features
- USB 3.0 x2/2.0 x2, Gb Ehernet, SATA x4, DisplayPort, Touch Screen
- Up to 2 SSD (2.5 in); AC or DC operation

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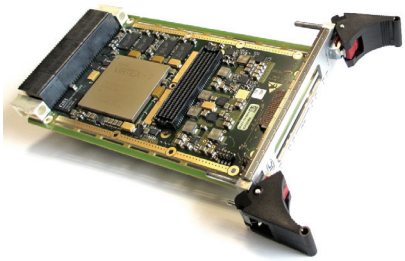
IC-FEP-VPX3c



The **IC-FEP-VPX3c** expands our Front End Processing family with a solution based on Xilinx Virtex-7 FPGAs (XC7VX690T, DDR3, QDRII+) to respond to seemingly insatiable bandwidth demand.

Designed for applications requiring a very high level of computing power in a compact 3U form factor, the IC-FEPVPX3c board offers the highest bandwidth with the lowest power consumption.

The IC-FEP-VPX3c mixed with the other building blocks of our 3U OpenVPX product ranges (Core i7 and PowerPC SBCs, Ethernet Switches & Routers, PCIe switch, FMC/XMC/PMC), running our Signal Processing Reference Design (including signal acquisition, Processing, DMA Engine, data storage, signal generation...), is the ideal platform for customers who want to streamline development by concentrating their efforts on their most critical tasks.

A MTCA.4 board with Virtex-7 and 2 FMC slots will be available soon. Please consult us.

FEATURES

- 1 Xilinx Virtex-7 XC7VX690T (other versions on demand)
- 2 banks of DDR3: 64-bit wide, 2GB each
- Optional QDRII+ 450MHz, 36-bit wide – up to 36 Mbits
- 128 MBytes of BPI NOR flash (bitstream storage)
- VPX Interfaces:
  - 4 4-lanes fabric ports on P1: 16 GTX/GTH (Fat Pipes A, B, C & D)
  - General purpose IOs on P2
  - 16 differential pairs (from FPGA)
  - 16 differential pairs (from FMC IOs connector)
- 1 FMC site:
  - 8 GTX/GTH (FPGA part number dependent)
  - 80 differential pairs
  - 4 reference clocks
- PIC µ-controller for System Management to VITA 46.11

The IC-FEP-VPX3c is a 3U VPX board compliant with 3U module definitions of the VITA 46.0 standard. It is available in air-cooled (1") and conduction cooled (0.8") versions compliant with VITA 47 classes.

Interface Concept | 800-445-6194
29000 Quimper, France • Ph: +33(0)2 98 573 030 • Fx : +33 (0)2 98 573 000

Contact: info@interfaceconcept.com

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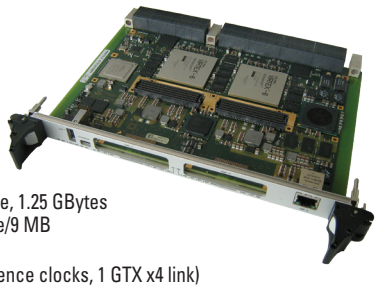
IC-FEP-VPX6a



The IC-FEP-VPX6a is a 6U VPX hybrid processing engine implementing two Virtex-6 FPGAs and one QorIQ processor, delivering a very high level of performance per watt.

With its PCIe advanced switch for a versatile coupling between the processing nodes and the backplane, the IC-FEP-VPX6a board expands the flexibility of the VPX high bandwidth serial interfaces. Two FMC mezzanine sites enlarge the adaptability of the board.

Delivered with a complete Signal Processing Reference Design (to empower customers to concentrate their efforts on their most critical tasks), the IC-FEP-VPX6a provides the ideal platform for radar, sonar, electronic warfare and other very high demanding digital signal processing applications.

A new version with Virtex-7 FPGAs will be available soon.
Feel free to consult us.

FEATURES

- 2 Xilinx Virtex-6: SX315T or SX475T (LX240T or LX550T possible), with each:
  - 2 banks of DDR3: 40-bit wide, 1.25 GBytes
  - 1 SRAM DDRII+: 18-bit wide/9 MB
  - 1 SPI flash (16 MBytes)
- 2 FMC slots (80 LVDS, 4 reference clocks, 1 GTX x4 link)
- 1 QorIQ processor P2020, 1GHz with:
  - 1 GB of DDR3 with ECC
  - 256 or 512 MBytes of NOR Flash
  - Optional Nand Solid-state Disk (eUSB module)
- 1 Spartan®-6 LX-45T (control Node) with 1 NOR flash (128 MBytes, for bistreams)
- VPX Interfaces:
  - 4 PCIe x4 port (from PCIe switch)
  - GTX ports (1 or 2 GTX x8 from each FPGAs)
  - 2 GTP (from Ctrl node FPGA)
- General purpose IOs:
  - 32 LVDS (16 from each FPGAs)
  - 32 differential pairs (16 from each FMC IOs connector)
  - GPIOs (from ctrl node FPGA)
  - 2 Ethernet ports (1000BT or 1000BX – from P2020
  - 1 RS485/RS232 port
  - 2 USB 2.0 ports
- PIC µ-controller for System Management (per VITA 46.11)

The IC-FEP-VPX6a is a VPX 6U board available in air cooled (1") and conduction cooled (0.8") versions

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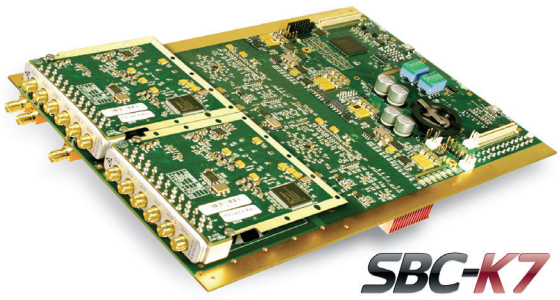
SBC-K7



The **SBC-K7** is an ideal platform for embedded instrumentation that combines an Atom PC running Windows/Linux/VxWorks with a Xilinx Kintex7 FPGA and an industry-compliant FMC IO site (HPC) plus a second FMC-compatble (LPC) site.

The CPU is a COM Express module featuring a single or dual core Intel Atom processor that is a fully compatible PC. The COM Express is optimized for low power, consuming only 6W, yet has Ethernet, USB, SATA, DisplayPort, touchscreen LCD, and PCI Express connectivity. The COM Express module is industry-standard, multi- sourced with a range of performance/power choices.

The FPGA computing core features the Xilinx Kintex 7 FPGA family, from K160T to K410T. The K410T provides 1540 DSP MAC elements operating at up to 500 MHz and 400K logic cells. The FPGA core has two memory banks, each of which is either up to 1GB LPDDR2 DRAM or 8MB QDRII SRAM.

FEATURES

- Embedded PC
  - Runs Windows/Linux
  - i7 CPU, 4 cores, 2.2 GHz, 8-16 GB or Atom CPU, 1 or 2 cores, 1.6GHz, 2GB
  - USB/1000 Ethernet/SATA/IEEE1588
  - Touchscreen LCD and DisplayPort support
  - Removable SDHC boot drive
- Small and Low Power
- FMC I/O site
- FPGA Computing Core
- Communications ports
- Timing Features
- Environmental ratings for -40 to 85C and 5g vibe

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Microsemi

www.microsemi.com/igloo2-fpga

IGLOO®2 FPGA

Microsemi's IGLOO®2 FPGAs, targeted at the cost-optimized FPGA market, integrate fourth generation flash-based FPGA fabric and high performance communications interfaces on a single chip. IGLOO2 devices offer best-in-class feature integration coupled with the lowest power, highest reliability and most advanced security in the industry. For cost-optimized FPGAs below 150K LEs, IGLOO2 provides a high level of I/O and SERDES integration – which is necessary for I/O expansion, bridging, system management and co-processing – allowing customers to use smaller devices for I/O expansion and bridging solutions. This, coupled with the need for only two power supplies and no external configuration devices, reduces overall system cost and board complexity.

In addition to many mainstream FPGA features, IGLOO2 is the only FPGA with hardened memory subsystem and only non-volatile and instant-on mainstream FPGA. The IGLOO2 FPGA family delivers the industry's lowest static power by providing 10 times lower static power than comparable FPGAs by utilizing a unique Flash*Freeze real-time power management mode. To protect valuable customer IP, the SEU-immune FPGA family includes state-of-the-art design security. Extended temperature ranges of up to 125C Tj are offered.

FEATURES

The IGLOO2 family delivers best-in-class integration, power, reliability & security and mainstream FPGA features including:

- highest number of GPIOs for any given density node for 5G SERDES FPGAs;
- highest number of 5G transceivers density;
- highest number of PCI compliant 3.3V I/Os in the industry; and
- highest number of PCIe endpoints.

Microsemi Corporation | 949-380-6100

Contact: sales.support@microsemi.com

Microsemi

www.microsemi.com

SmartFusion®2 SoC FPGAs

Microsemi's SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) family features the only devices that address important fundamental requirements for advanced security, high reliability and low power in critical industrial, military, aviation, communications and medical applications. SmartFusion2 integrates inherently reliable flash-based FPGA fabric, a 166 megahertz (MHz) ARM® Cortex™-M3 processor, advanced security processing accelerators, DSP blocks, SRAM, eNVM and industry-required high-performance communication interfaces all on a single chip.

Microsemi's programmable logic solutions are used extensively in military, aviation and space applications due to their reliability and protection against Single Event Upset (SEU) occurrences, which can cause binary bits to change state and corrupt data and cause hardware malfunction. Industrial and medical safety markets are also requiring SEU protection as a vital requirement for their applications.

FEATURES

- Highest reliability, most secure, lowest power FPGA
- Up to 150K LEs with 5Mbit SRAM and 4.5Mbit NVM
- SEU immune zero FIT flash FPGA configuration cells
- Hard 667 Mbps DDR2/3 controllers with SECDED
- Industry's lowest static power 10mW during operation on the 50K LUT device
- 1 mW standby power in Flash*Freeze real-time low power state

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Contact: sales.support@microsemi.com

Annapolis Micro Systems

www.annapmicro.com

CoreFire

Develop your application very quickly and easily with our **CoreFire™ FPGA Application Builder**, which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field.

Use CoreFire's graphical interface to drag and drop library elements onto the design window. Modify your input and output types, numbers of bits, and other core variables by changing module parameters with pull-down menus. The modules automatically provide correct timing and clock control. Insert debug modules to report actual hardware values for hardware-in-the-loop debugging. Hit the Build button to check for errors and as-built core sizes and to build an encrypted EDIF file. Use the Xilinx ISE tool to place and route each FPGA design. Modify and use the jar file or the C program created by the CoreFire Build to load your new file into your WILDSTAR and I/O card hardware. Use the CoreFire Debugger to view and modify register and memory contents in the FPGA and to step through the dataflow of your design running in the real physical hardware.

Our extensive IP and board support libraries contain more than 1,000 proven, reusable, high-performance cores, including FIR and CIC filters, a channelizer, and the world's fastest FFT. We support conversion between data types: bit, signed and unsigned integers, single precision floating point, integer and floating point complex, and arrays. A few of the newly added array cores include array composition and decomposition; slice, parallelize, serialize, repack, split, merge, reorder, rotate, and concatenate transformations; matrix math, sliding windows, and convolutions.

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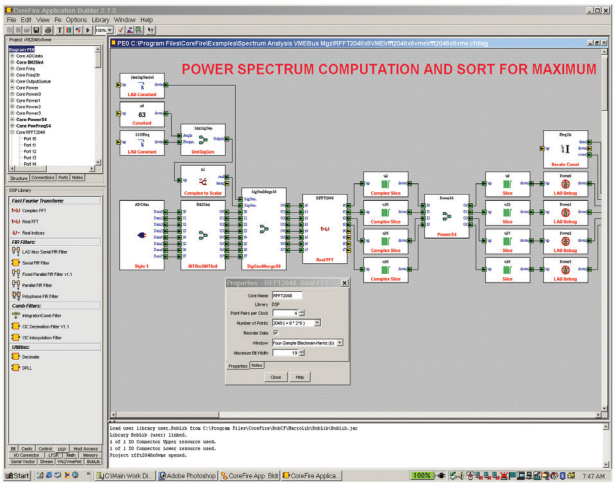

FEATURES

- Dataflow-based – automatically generates intermodule control fabric
- Drag-and-drop graphical interface
- Work at high conceptual level – concentrate on solving algorithmic problems
- Hardware-in-the-loop debugging
- More than 1,000 modules incorporate years of application experience
- Reduce risk with COTS boards and software
- Save time to market
- Save development dollars
- Easily port completed applications to new technology chips and boards
- Training and custom application development available
- Achieve world-class performance; WILD solutions outperform the competition
- Annual node locked or networked license; includes customer support and updates

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Development Tools: Prototyping

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HAPS-70: FPGA-Based Prototyping System

HAPS-70 series is an easy-to-use and cost-effective FPGA-based prototyping system. Enhancements to the HAPS system technology, as well as the use of the latest Xilinx Virtex®-7 FPGAs, provide designers using the HAPS-70 series with superior capacity, performance, and advanced use modes. The HAPS-70 series accelerates early software development, hardware/software integration and system-level validation at near-real-time run rates, using at-speed real-world interfaces.

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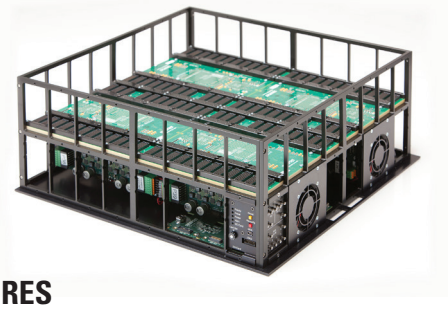

FEATURES

- Modular system architecture scales from 12-144M ASIC gates to accommodate a range of design sizes, from individual IP blocks to processor subsystems to complete SoCs
- Enhanced HapsTrak 3 I/O connector technology with high speed time-domain multiplexing delivers up to 3x performance improvement in data throughput over traditional pin multiplexing
- System definition and bring-up utilities speed hardware assembly and ensure the prototype's electro-mechanical integrity
- Design planning tools reduce time-to-prototype by 2-3 months, streamlining the transition from block level IP validation to full system integration
- Improve debug efficiency with 100x greater visibility
- Advanced use modes including co-simulation, transaction-based verification, and hybrid prototyping
- HAPS-70 FPGA-based prototyping systems are available in nine model variants

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ePC-K7

The **ePC-K7** is a user-customizable, turnkey embedded instrument that includes a full Windows/Linux PC and supports a wide assortment of ultimate-performance FMC modules. With its modular I/O, scalable performance, and easy to use PC architecture, the ePC-K7 reduces time-to-market while providing the performance you need.

- *Distributed data acquisition*
- *Uniquely customizable*
- *Remote or local operation*
- *Continuous data streaming*
- *Rugged – SSD boot drive support in a compact, rugged 8 x 11" footprint*
- *Download data sheets and pricing now!*

FEATURES

- Combines an industry-standard COM Express CPU module with dual FMC I/O modules in a compact, stand-alone design
- Programmable Kintex-7 325/410 and Spartan-6 FPGAs
- Small form factor: 5" H x 8" W x 11" D
- Conduction cooled design: Fins or cold-plate
- Stand-alone operation: Able to operate headless, booting from SSD
- Windows, Linux OS support
- Dual VITA 57 FMC I/O module sites. Add anything from RF receivers to industrial control modules.

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micro-line C641x DSP/FPGA Boards

The micro-line series of embedded DSP/FPGA boards provides embedded systems developers with a tightly integrated suite of programmable DSP, FPGA, and I/O resources in small, stand-alone capable board formats.

micro-line C6412Compact and **C641xCPU** DSP/FPGA boards target high-performance integer DSP applications, using the Texas Instruments TMS320C6410, TMS320C6412, TMS320C6413, and TMS320C6418 DSPs.

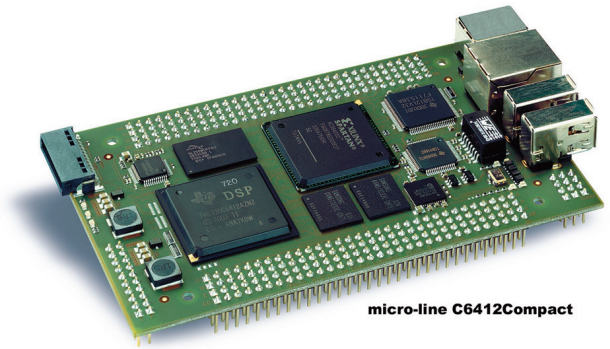
The micro-line C6412Compact combines a powerful 720 MHz TMS320C6412 DSP processor, up to 128 MB SDRAM, 8 or 32 MB flash ROM, and a high-density 1M gate or 4M gate Spartan-3 FPGA. The optionally programmable FPGA greatly expands processing and interfacing possibilities. Two independent 400 Mbps 1394a FireWire interfaces are included, enabling simultaneous high-bandwidth video-in and video-out for a completely integrated video processing system. A 64-bit bus connects the DSP, FPGA, SDRAM, and FireWire resources. Onboard USB 2.0 and 10/100BASE-Tx Ethernet interfaces round off the impressive feature set available on the C6412Compact.

The C641xCPU family of boards features a smaller (98 mm x 67 mm footprint) and leaner configuration, with up to 64 MB SDRAM, 8 MB FLASH ROM, and a high-density 500K gate, 1M gate, or 1.6M gate Spartan-3E FPGA.

Optional Analog I/O daughtercards can also be used with the C6412Compact and C641xCPU boards:

ORS-114 (14-bit A/D/A)
- 2-ch A/D 65 MSps; 2-ch D/A 125 MSps
- 4-ch A/D 65 MSps; 4-ch D/A 62.5 MSps

ORS-116 (16-bit A/D/A)
- 12-ch A/D 250 KSps; 12-ch D/A 100 KSps


micro-line C6412Compact

micro-line FEATURES

› C6412Compact:
- 720 MHz TMS320C6412 integer DSP
- 1M gate or 4M gate Spartan-3 FPGA; up to 211 configurable I/O pins
- Up to 128 MB SDRAM
- Up to 32 MB flash ROM for DSP and FPGA boot code, as well as non-voltatile parameter/data storage
- Two independent IEEE1394a FireWire interfaces for streaming data in/out simultaneously
- 10/100BASE-Tx Ethernet interface
- USB 2.0 and RS-232 interfaces
- External access to DSP Processor I/O interfaces: 64-bit EMIF, XF0/1 pins, Timer input/output pins, McBSP ports, I2C, and 16-/32-bit HPI
- 120 mm x 72 mm footprint; ISO9001:2000 accredited production and CE certification

› C641xCPU:
- 400 MHz TMS320C6410, 500MHz TMS320C6413 or 500 MHz TMS320C6418 integer DSP
- 500K gate, 1.2M gate, or 1.6M gate density Xilinx Spartan™-3E FPGA; up to 98 configurable digital I/O pins
- Up to 64 MB SDRAM
- 8 MB flash ROM for DSP and FPGA boot code, as well as non-voltatile parameter/data storage
- RS-232 interface
- External access to DSP Procesor I/O interfaces: 32-bit EMIF, XF0/1 pins, Timer input/output pins, McASP and McBSP ports, I2C, and HPI
- 98 mm x 67 mm footprint; ISO9001:2000 accredited production and CE certification

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micro-line C6713 DSP/FPGA Boards

The micro-line series of embedded DSP/FPGA boards provides embedded systems developers with a tightly integrated suite of programmable DSP, FPGA, and I/O resources in small, stand-alone capable board formats.

micro-line C6713Compact and **C6713CPU** DSP/FPGA boards target high-performance floating-point DSP applications, using the powerful Texas Instruments TMS320C6713 DSP.

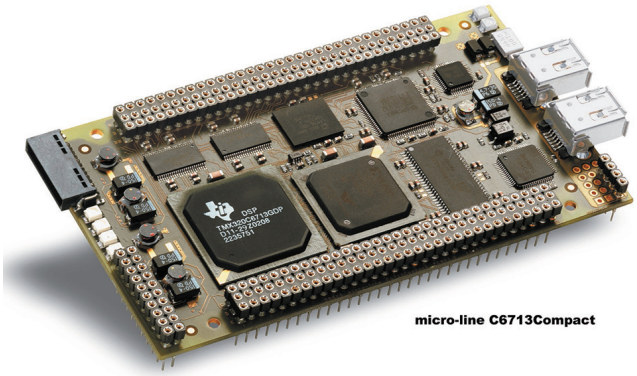
The C6713Compact combines a powerful 300 MHz TMS320C6713 floating-point DSP processor, up to 128 MB SDRAM, 8 MB boot program ROM and an on-board, high-density Xilinx Spartan-6 LX or Virtex-II FPGA (optionally programmable). The FPGA greatly expands processing and hardware interfacing options. A 400 Mbps IEEE 1394a FireWire interface is also included onboard, for communications with other embedded DSP resources, cameras, sensors, and PCs. Software APIs are available to utilize the FireWire interface for general purposes, video frame capture from cameras, and data storage to hard drives and CompactFlash memory.

The C6713CPU offers a smaller (98 mm x 67 mm footprint) and leaner configuration, which has up to 64 MB SDRAM, and 2 MB flash ROM, along with a high-density 400K gate or 1M gate Spartan-3 FPGA.

Optional Analog I/O daughtercards can also be used with the C6713Compact and C6713CPU boards:

ORS-114 (14-bit A/D/A)
- 2-ch A/D 65 MSps; 2-ch D/A 125 MSps
- 4-ch A/D 65 MSps; 4-ch D/A 62.5 MSps

ORS-116 (16-bit A/D/A)
- 12-ch A/D 250 KSps; 12-ch D/A 100 KSps


micro-line C6713Compact

micro-line FEATURES

› C6713Compact:
- 300 MHz TMS320C6713 floating-point DSP
- Spartan 6 (LX45, LX75, LX100 or LX150) or Virtex-II (250kGate or 500kGate) FPGA; up to 160 configurable digital I/O pins
- Up to 128 MB SDRAM
- 8 MB flash ROM for DSP and FPGA boot code, as well as non-voltatile parameter/data storage
- Onboard 400 Mbps IEEE1394a FireWire interface
- RS-232 interface
- External access to TMS320C6713 DSP I/O interfaces: 32-bit EMIF, XF0/1 pins, Timer input/output pins, McASP and McBSP ports, I2C, and HPI
- 120 mm x 67 mm footprint; ISO9001:2000 accredited production and CE certification

› C6713CPU:
- 300 MHz TMS320C6713 floating-point DSP
- 400K gate or 1M gate Spartan-3 FPGA; up to 96 configurable digital I/O pins
- 64 MB SDRAM
- 2 MB flash ROM for DSP and FPGA boot code, as well as non-voltatile parameter/data storage
- RS-232 interface
- External access to TMS320C6713 DSP I/O interfaces: 32-bit EMIF, XF0/1 pins, Timer input/output pins, McASP and McBSP ports, I2C, and HPI
- 98 mm x 67 mm footprint; ISO9001:2000 accredited production and CE certification

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Contact: sales@traquair.com

Annapolis Micro Systems

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Four Channel Clock Synchronization Board

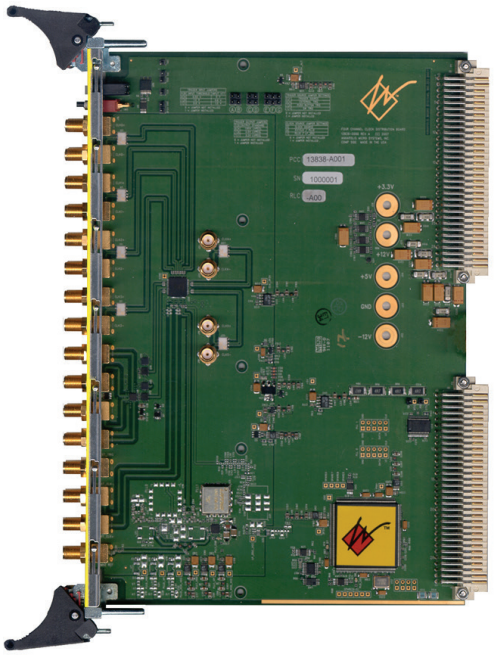
The **Four Channel Clock Synchronization Board** distributes a common clock and synchronized control signal triggers to multiple cards in the system. This 6U VME64x/VXS board provides four high-speed, ultra-low jitter, ultra-low skew differential bulkhead mounted clock outputs, two ultra-low skew differential vertical SMA on-board clock outputs, and four ultra-low skew and clock synchronized single-ended bulkhead mounted control signal triggers.

A jumper set at board installation time or via optional P2 Serial Port determines which one of the two installed clock sources is active. Manufacturing options for Clock Source 0 are Single Ended or Differential External Clock, a PLL ranging from 700 MHz to 3 GHz with an On-board Reference Oscillator, or a PLL ranging from 700 MHz to 3 GHz with a 10 MHz External Reference. Manufacturing options for Clock Source 1 are a PLL ranging from 700 MHz to 3 GHz with an On-board Reference Oscillator, a PLL ranging from 700 MHz to 3 GHz with a 10 MHz External Reference or an On-Board Low Frequency Oscillator ranging up to 800 MHz.

The four control trigger outputs can originate from a high-precision external source via front panel SMA, from a manual pushbutton on the front panel, or from software via an optional Backplane P2 Connector Serial Port. These trigger outputs are synchronized to the distributed clock to provide precise output timing relationships.

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based boards and processing for RADAR, SONAR, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customer's applications succeed. We offer training and exceptional special application development support, as well as more conventional support.



FEATURES

- Four Synchronized Differential Front Panel Clock Outputs up to 3 GHz with Typical Skew of 5 ps
- Ultra-low Clock Jitter and Phase Noise – 275 Fs with 1,280 MHz PLL and external 10 MHz Reference
- On-board PLLs Manufacturing Options provide Fixed Frequencies of 700 MHz to 3 GHz, Locked to Internal or External Reference
- On-board Low Frequency Oscillator provides Fixed Frequencies up to approximately 800 MHz
- Four Synchronized Trigger Outputs, always Synchronized with the Output Clock, with Typical Skew of 5 ps
- Jumper Selectable Trigger Output Levels of 3.3 V PECL, 2.5 V PECL, or 1.65 V PECL
- Source Trigger from Front Panel SMA, Pushbutton, or Optional P2 Serial Port
- Cascade boards to provide up to 16 sets of outputs
- Compatible with standard VME64x and VXS 6U backplanes
- Universal clock input supports wide range of signal options, including signal generator sine wave
- Differential clock input permits multiple standards including: LVDS, 3.3 V PECL, 2.5 V PECL, and 1.65 V PECL
- Clock and Trigger Outputs Compatible with all Annapolis Micro Systems, Inc. WILDSTAR™ 2 PRO I/O Cards and WILDSTAR™ 4/5 Mezzanine Cards

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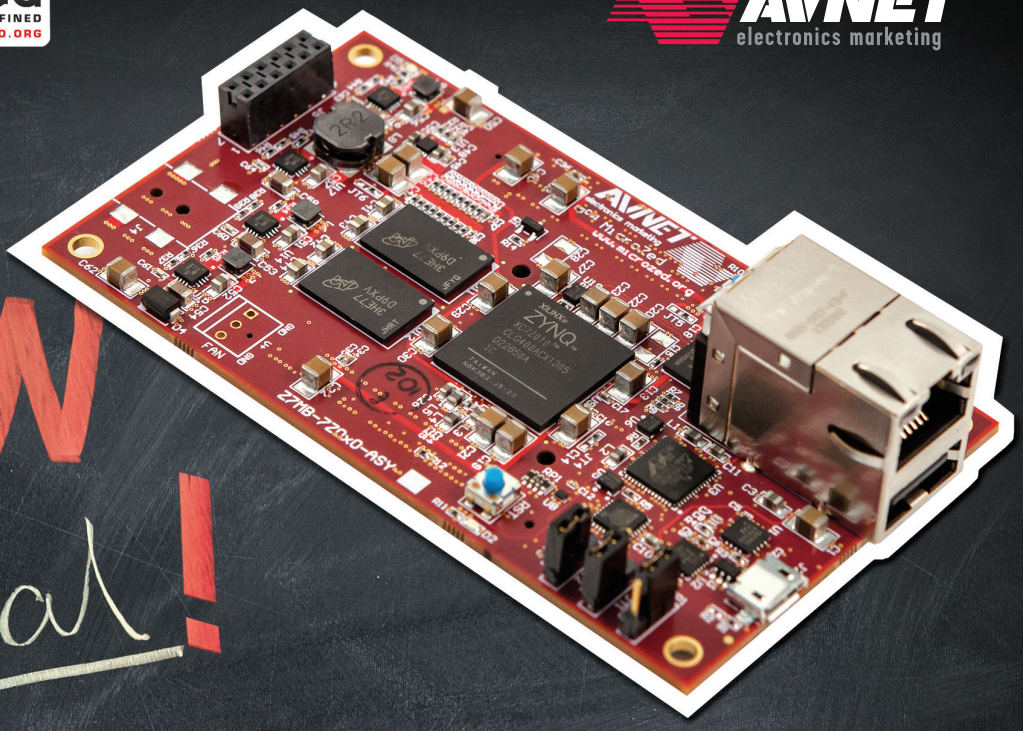

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- √ Low-cost development tool
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- √ Out-of-the-box Linux support
- √ Easy migration from prototype to production

ZYNQ®

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MicroZed™ is a low-cost development board based on the Xilinx Zynq®-7000 All Programmable SoC. Its unique design allows it to be used as both a stand-alone evaluation board for basic SoC experimentation, or combined with a carrier card as an embeddable system-on-module (SOM). This combined stand-alone/SOM approach can quickly move a design idea from concept to production, making MicroZed the ideal platform for SoC based applications. MicroZed is supported by a community website where users can download kit documentation and reference designs as well as collaborate with other engineers also working on Zynq designs.

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