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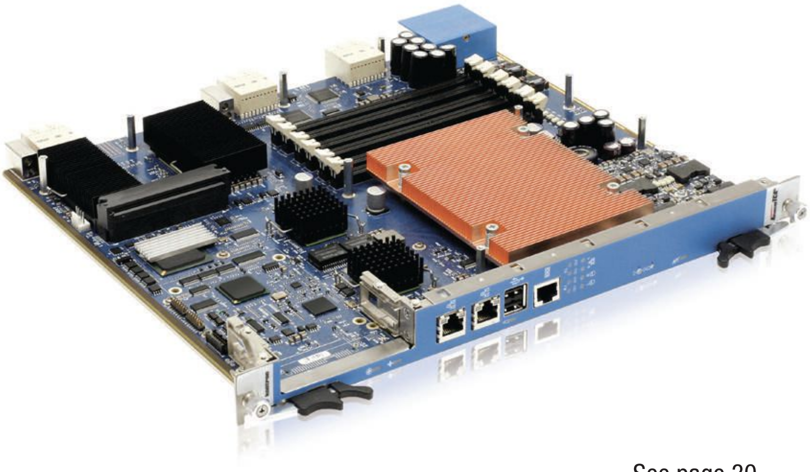

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Next Stop, 40G

2011 Buyer's Guide

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FEATURES

2011 BUYER'S GUIDE

COVER → Gene Juknevicius, Senior Architect & Technologist, GE Intelligent Platforms, explains in this issue that "a mandatory first step to 40G is an infrastructure that includes 40G-capable backplanes, connectors, and hub blades." Doubtless many of the vendors featured in this Buyer's Guide issue will be playing key roles in the transition to 40G as our appetite for bandwidth-gobbling apps continues to grow.

Shown on the cover is the Adax PacketRunner, an intelligent AdvancedTCA carrier blade with an onboard Cavium OCTEON 5650 multicore processor.

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EDITOR'S FOREWORD

Reaching the Summit

By JOE PAVLAT

The fifth annual AdvancedTCA/MicroTCA Summit was held last month in Santa Clara, CA. Once again, Lance Leventhal and his crew at Conference ConCepts put on a great event. There were some great tutorials and keynotes, including speeches by senior officials involved with military procurement and its intricacies. Ray Larsen from the Stanford Linear Accelerator Center explained how "Big Science" is adopting AdvancedTCA and MicroTCA. Particle accelerators and astronomy applications such as the large synoptic survey telescope were among the applications Ray covered. All of the presentations may be viewed at: http://www.advancedtcasummit.com/English/Conference/Proceedings_Chrono.html

Thirty-three exhibitors showed their latest products, and I was impressed with the maturity of AdvancedTCA and the sophistication of its vendor base. Everyone was talking about the move from 10 gigabits/second data transfers to 40 gigabits/second, which is viewed as key if AdvancedTCA is to dominate the next generation networks that will be rolled out over the next few years. And the analysts seem to think that it will.

Latest PICMG workshop on interoperability

The most recent PICMG Interoperability Workshop, the organization's twenty-first, was held in Germany in September and featured the testing of a variety of first generation 40G products. Early 2011 will see the completion of the PICMG standard that formalizes the design guidelines. But AdvancedTCA wasn't the only technology on display at the Interoperability Workshop. A wide variety of MicroTCA and AdvancedMC modules were shown, and BAE Systems displayed a hardened, conduction-cooled MicroTCA system designed for mil/aero applications that conforms to the PICMG specification now in final member review.

Fastest-growing segment

Richard Dean, who is Program Manager for Embedded Hardware at VDC Research, the widely respected analyst firm, delivered one of the Summit's more interesting presentations. His detailed forecast has the merchant market for AdvancedTCA CPU blades reaching $400M next year and $600M by 2013. He predicts a CAGR of 22 percent annually, making AdvancedTCA the fastest growing segment of the embedded computer market. It is worth noting that these numbers are for CPU boards only – mostly Intel based – and do not include chassis, switches, DSP boards, or packet processing boards. This suggests that the entire value of annual system sales is already well over the one-half-billion dollar mark and growing nicely. He believes about 80 percent of the market now is telecom and communications, with mil/aero occupying around 15 percent. Another interesting number Richard presented was the size of the CompactPCI CPU board market, which exceeds $500M annually and is declining quite slowly. He expects CompactPCI to remain a very good market for years to come and, again, this number does not include chassis, I/O cards, switches, etc.

Summit organizers added a new technology to the Summit this year, "COM Express Day," featuring products and presentations from leading suppliers. The wide variety of applications using COM Express is impressive, and the range of apps includes communications, industrial control, displays, and mil/aero.

One of the highlights of the Summit for me was the opportunity to present the annual Industry Achievement Award to my colleague and friend Stephen Dow, who is President of Emerson Network Power's Embedded Computing Division. Stephen also gave a very upbeat keynote presentation on AdvancedTCA and the challenges it faces. He believes AdvancedTCA is already a success, and will continue to be one.

Speaking of 40 gig ATCA, as it is generally called, two articles in this issue go into considerable detail on the subject. The article by GE Intelligent Platforms explains some of the applications for 40G AdvancedTCA, and an article by Emerson dives into some of the technical challenges that must be solved and are being solved.

Wire-speed packet processing is a key ingredient for IP-based networks, and much has been written about it. In his article, Charlie Ashton from 6WIND presents another angle, using multicore Intel processors for high-speed packet processing.

Joe Pavlat

Joe Pavlat, Editorial Director

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FEATURE

AdvancedTCA transitions to 40G

Gene describes the backplane, connector, and hub blade must-haves for transitioning to 40 Gigabit Ethernet, then considers how packet processing blades and other payload blades will capitalize on the passage to 40G AdvancedTCA architecture.

By Gene Juknevicius

Everyday experiences, such as using an Internet-connected mobile phone or IPTV to handheld devices, give us insight into the data bandwidth explosion that telecom networks, and especially wireless networks, are experiencing. This customer-side demand is having a pass-the-magnet-over-the-iron-filings effect on key 40G AdvancedTCA architecture elements, gathering them together.

Among these elements are the AdvancedTCA backplane and connectors. The PICMG 3.0 AdvancedTCA specification defines board-to-backplane connectivity in terms of channels. Each channel consists of eight differential pairs, four for transmit and four for receive. This channel definition nicely accommodates the 10/100/1000BASE-T interface used for the Base Channel. In the case of a 10G Fabric Channel, XAUI (also known as 10GBASE-KX4), four lanes in parallel operating at 3.125 GHz each are utilized.

Four lanes operating at 10G each will supply the necessary bandwidth for transitioning to 40G interconnect. IEEE's timing was perfect: This past summer, it released the IEEE 802.3ba specification in which 10GBASE-KR and 40GBASE-KR4 interfaces are defined. 40GBASE-KR4 is defined to reach 1 meter on the backplane, positioning it for AdvancedTCA backplane connectivity.

While increasing frequencies from 3.125 GHz to 10.3125 GHz is no small feat, AdvancedTCA connector vendors came through with ATCA Zone 2 connectors rated for 10.3125 GHz and higher signaling. Although the new high-speed connector is not footprint-compatible with AdvancedTCA blades, it is able to mate with older, lower-speed connectors as well as new, higher-speed connectors. The interoperability this affords is important, enabling a gradual upgrade path and an ecosystem in which 10G AdvancedTCA blades can be plugged into a new 40G backplane, and new 40G blades can be plugged into older 10G backplanes.

Too much for off-the-shelf switch silicon to handle?

The next key element of the 40G AdvancedTCA architecture is the AdvancedTCA hub, also known as a switch blade. The AdvancedTCA specification defines a chassis with up to 16 slots; therefore, the AdvancedTCA hub would need to have connections to a maximum of 14 AdvancedTCA node blades and a redundant hub – 15 ports in total. Simple math shows that for 40G aggregate throughput becomes 600 Gbps. Add to this two external 40G ports and some extra on-board connectivity and it easily reaches 700 Gbps. That is a lot of bandwidth for standard off-the-shelf Ethernet switch silicon. Only recently did the silicon vendors begin offering products that can approach such bandwidth in a single device.

Space and power on AdvancedTCA designs is limited, so ideally the Ethernet switch silicon would include built-in physical interface devices (SerDes) that would connect directly to the backplane. Furthermore, in order to support backward compatibility, each Fabric Channel needs to be capable of supporting all of the following interface types:

- 1x 40GBASE-KR4 (typical 40 Gbps connection)
- 4x 10GBASE-KR (a trunk of four 10 Gbps connections)
- 1x 10GBASE-KX4 (backward compatible, 10 Gbps XAUI connection)
- 4x 1000BASE-KX (backward compatible, four 1 Gbps connections)

A changing connectivity role

Now that speed and connectivity have been covered, it is time to consider switching functionality. Historically, AdvancedTCA hubs have played a somewhat simple in-box connectivity role. These older switches mostly performed Layer-2 switching functions, with a little Layer-3 functionality, also know as IP switching or routing. With migration to 40G AdvancedTCA architecture, expectations for the AdvancedTCA hub are beginning to change dramatically. 40 Gbps is a lot of bandwidth and can easily overrun end point devices as well as the buffer space of the switch itself.

Consider the following calculation. Say there are only two blades communicating at 40 Gbps via a switch. If the receiving blade stops receiving traffic and issues an XOFF flow control command, it takes about 2 milliseconds to completely fill the 10 MB buffer space typically available on switch silicon. Extrapolate this to a complete 16-blade system and the problem becomes clear. When congestion occurs, Ethernet drops packets. This is not good. At the very least, the user needs some control over which packets are dropped. Also, it would be desirable to be able to classify packets into priority classes and have flow control that operates on a per class basis, as opposed to as happens with standard XOFF.

Although priority flow control and policing are becoming standard features in Ethernet switch silicon, the switch's ability to classify packets and take a specific action accordingly needs to be analyzed very carefully. Ideally, the packet classifier would be very flexible, with the ability to look deep into the packet and into any bit field within the packet header in order to make appropriate decisions. Imagine that you want to identify Voice over IP packets and give them higher priority. And, you want to identify streaming video and prioritize these packets accordingly. Next, you want to mark packets that are related to a routine backup storage application as low priority – making them candidates for packet drop when congestion occurs. Such packet classification and congestion management is only the first step in a comprehensive congestion management scheme. More advanced features, such as Quantized Congestion Management or Virtual Output Queuing, will enhance the scheme.

Scalability economics

Flexibility in a 40G hub is yet another important requirement. In the previous paragraphs, it was shown how the 40 Gbit bandwidth required by each slot quickly adds up. Switching silicon must be able to handle high bandwidth and be ready to scale down performance to reach required price/performance points. High-end switching silicon is expensive. What if a particular application only needs eight or 10 slots that are capable of sustained 40 Gbps throughput? While it is desirable that the remaining slots be able to connect using a 40G interface, the application may never use these ports at the highest data rate. In this case, an AdvancedTCA hub design that is capable of accommodating switch silicon versions with different aggregate throughput and is priced accordingly makes sense. This option is especially attractive if the switch configuration and management software can be identical between versions. The system designer can start out low and grow hub capacity as need grows.

I/O flexibility

AdvancedTCA hub I/O requirements vary widely. For example, some applications require front I/O, some rear I/O, and others need an added x86 processor as the AdvancedTCA System Controller. Then there are those applications that must avoid Rear Transition Module (RTM) use to save costs and those with Deep Packet Inspection (DPI) or encryption/decryption demands on a few uplink ports. Still others are looking to have an additional Traffic Manager added to the switch. One way to address this wide range is with two or more AdvancedMC module slots on the hub that are connected using high data rates to the Fabric and Base switches. This approach adds flexibility and can open up multiple avenues for future expandability.

As noted earlier, a large number of additional ports are expected from the Ethernet switch silicon, which is already oversubscribed with connections to the blades. The idea presented is that all this flexibility can be made possible if switch silicon supports a larger number of interfaces when compared to the maximum throughput that it can sustain. Not all of these ports will be used at the same time, but it is beneficial to make configuration decisions dynamically without committing to purchasing one or the other AdvancedTCA hub assembly options up front.

A mandatory first step to 40G is an infrastructure that includes 40G-capable backplanes, connectors, and hub blades. Two such hubs can be used to validate communication at 40G speeds across the backplane. Even though the rest of the AdvancedTCA blades may be 1G or 10G, the chassis will be ready for gradual migration to a 40G architecture.

Next stop, 40G

When we consider payload blades, the question to ask is not "which blades need 40G?". Rather it is "which blades will need more than 10G bandwidth?". As soon as the blade bandwidth requirement tops 10G, there is little choice other than moving to 40G.

Packet processing blades, for example, are specifically designed and optimized for processing high packet rates and can benefit from bandwidth larger than 10G. Packet processing blades are typically used in applications such as gateways, soft switches, firewalls, network intrusion detection systems, DPI and lawful intercept devices, and network test and monitoring equipment. A typical AdvancedTCA chassis would have a few packet processing blades operating in parallel. In this case, the 40G hub must analyze incoming packets and steer them to an appropriate packet processing blade. Note that packet steering decisions will usually involve packet parameters above and beyond the IP and MAC addresses typically used to make switching and routing decisions (see Figure 1).

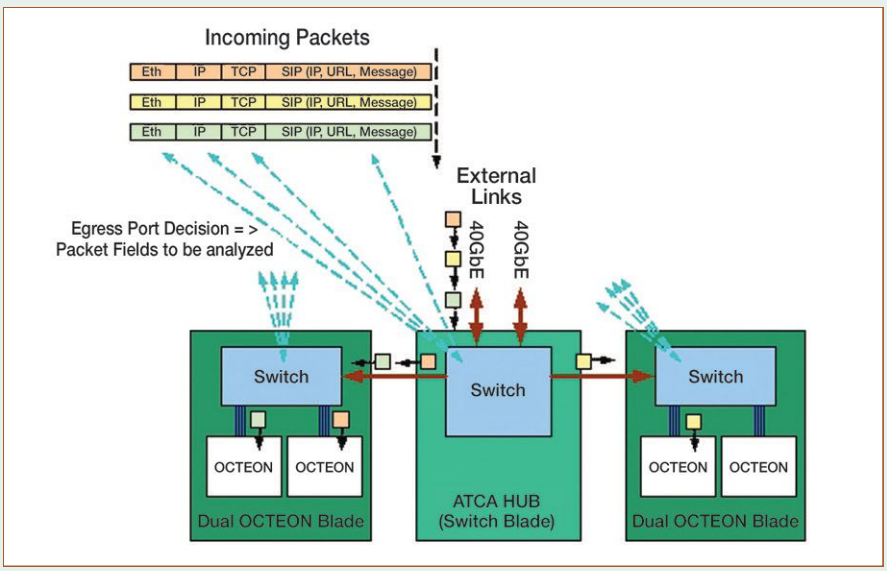

Figure 1 | **SIP packets are steered by each Ethernet switch based on L-2, L-3, L-4, and SIP information.**

Furthermore, typical packet processing blades have two or more processing silicon devices; consequently, the packet processing blade itself will have its own Ethernet switch. This switch will have to further analyze the packet and make its own decision as to which processor forwards the packet.

Notice that now there is an Ethernet switch on the hub blade directly connected to Ethernet switches on the AdvancedTCA node blades. Although – due to Ethernet interoperability – switches from multiple manufacturers interoperate, having switches from the same vendor enables additional, proprietary functions. These functions can optimize packet parsing, lookup, and decision-making. They can reduce packet switching latencies, optimize switch packet buffer memory usage, and more efficiently communicate congestion and packet queue status.

Along with a number of purpose-designed silicon devices, such as Cavium Networks' OCTEON processors, mainstream processors such as the x86 are also being positioned for packet processing tasks.

Other blades, such as x86 processor blades used for video caching or video on demand, for example, will also benefit from data rates above 10G. Historically, x86 processors were not very good at handling high I/O data rates. Today, significant improvements have been made in this area. We can measure most bottlenecks by how many packets per second a specific architecture can process. Expressing performance limitation in packets per second draws a clear line from increased packet size to greater overall data throughput. Video server and other applications that operate with very large packets are the leading candidates to profit from the transition to a 40G AdvancedTCA architecture.

Mixing and matching 10G and even 1G blades with 40G blades (Figure 2) is possible with the AdvancedTCA architecture.

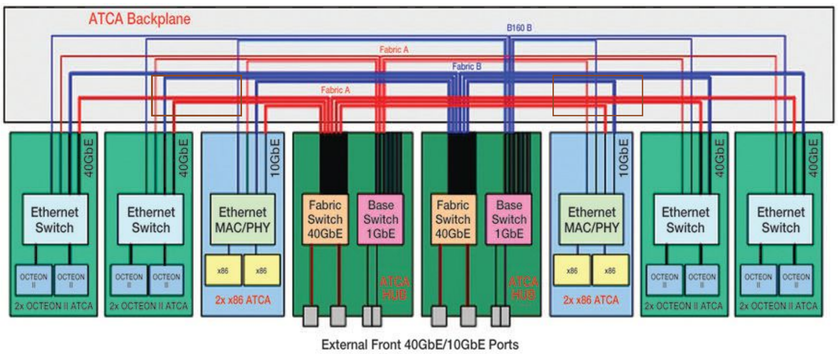

Figure 2 | AdvancedTCA system interconnects and a mix of 40G and 10G AdvancedTCA blades.

Customer demand and required technology forces have aligned to make the transition to 40G happen, and inherent backward compatibility with 10G and 1G products will aid this transition, enabling gradual upgrades and a grow-as-you-go model.

Gene Juknevicius is Senior Architect & Technologist, GE Intelligent Platforms. He has participated in the PICMG AMC, and MicroTCA committees, is currently an active member of the SCOPE Alliance, and is responsible for new product definition and architecture at GE Intelligent Platforms. He received his M.S. degree in Electrical Engineering from Stanford University.

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FEATURE

Designing for 40G AdvancedTCA

By Dr. Mathias Hellwig

Dr. Hellwig previews some of the challenges (which will be described in greater detail in a forthcoming Emerson Network Power Embedded Computing white paper) that crop up when 40 Gbps rather than 10 Gbps becomes the system interconnect.

Hardware design – Bit Error Rate (BER)

Signal integrity requirements affect the Bit Error Rate (BER), defined as the ratio of the total number of transmitted bits versus the number of incorrect received bits. Most standard protocols such as Ethernet require a BER of 10-12.

For binary symmetrical channels the BER can be calculated as described in Figure 1 based on the error probability of a transmission of an individual bit.

Bit errors can have several causes, including noise, attenuation, interference, and distortion.

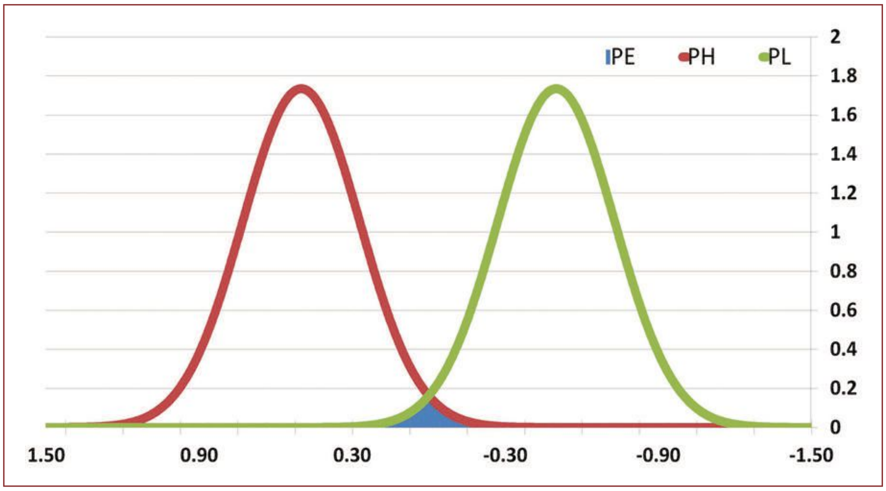

Figure 1 | Error probability of a binary symmetrical channel

Channel modeling – PCB effects

The increased signal speed associated with 40G AdvancedTCA has physical effects that must be considered to achieve an accurate design.

The first one is referred to as "skin effect" and can be modeled as a resistance, which is proportional to the square root of the frequency and inverse proportional to the width of the trace line.

$$P_e = \frac{1}{2}\operatorname{erfc}\left(\frac{1}{\sqrt{2}}\left[\frac{m_H - m_L}{\sigma_H + \sigma_L}\right]\right)$$

Equation 1 | Parameter specification for a printed circuit board design with a line speed less than 1 gigabit

Another, more important factor is the material-dependent relative permittivity. For a PCB design below 1 gigabit line speed, the parameter is specified as $\varepsilon_r \approx 4$ which is sufficiently accurate at that speed. For higher data rates, however, this approach is no longer adequate and has to be considered as more complex as shown in Equation 1.

Considering these two physical phenomena, skin effect and variation of the relative permittivity, it becomes clear that for a 40 Gbps system things need to change with respect to material selection and design methodology.

Design effects

Modern high-speed designs abandon the use of buses as interconnects because of skew and Electromagnetic Compatibility (EMC) issues, and focus primarily on serial interconnects. Skew issues for parallel interconnects are resolved at the protocol level.

The current return path in the reference planes needs to be carefully investigated, because gaps or split ground in the reference plane of the transmission path will create Electromagnetic Interference (EMI), resonances, and increased cross-talk.

Simulation

Three levels of abstraction can be distinguished: the more abstraction, the higher the simulation performance as shown in Table 1.

(1) Field level simulators are a finite element field solver for fields. The tools can calculate field in the time or frequency domain, based on geometries and material characteristics, which can be non-linear and anisotropic in conductivity, permittivity, or permeability. The results can be visualized or asserted as an n-port S-parameter matrix.

(2) The next level of simulation abstracts from material properties and any geometric shapes. The simulation deals with equivalent circuits, distributed transmission lines for strip and microstrip-lines, s-parameter sets, and semiconductor devices. It is able to calculate circuits with linear and non-linear behavior. Mainly the receiver and transmitter circuits show non-linear behavior.

(3) Finally, the highest level of abstraction for signal integrity is the link-level simulation. In the simulation all circuits are considered as linear circuits, and algorithms model the digital part of the receiver and transmitter. The tools are vendor-specific and provided by the SerDes vendors, because the models for the receiver and transmitter contain their considerable IP.

The result of circuit- or link-level simulation can be displayed either as a waveform of voltages, usually as differential signals, or as an eye pattern. Eye patterns are constructed out of simulated or measured waveforms and show parametric information about the signal. The waveform is sliced in time intervals of two-bit periods for each bit and then all slices are superimposed into one diagram. Figure 2 shows an eye diagram with a huge number of superimposed slices, typically in the range of 100,000 or more slices.

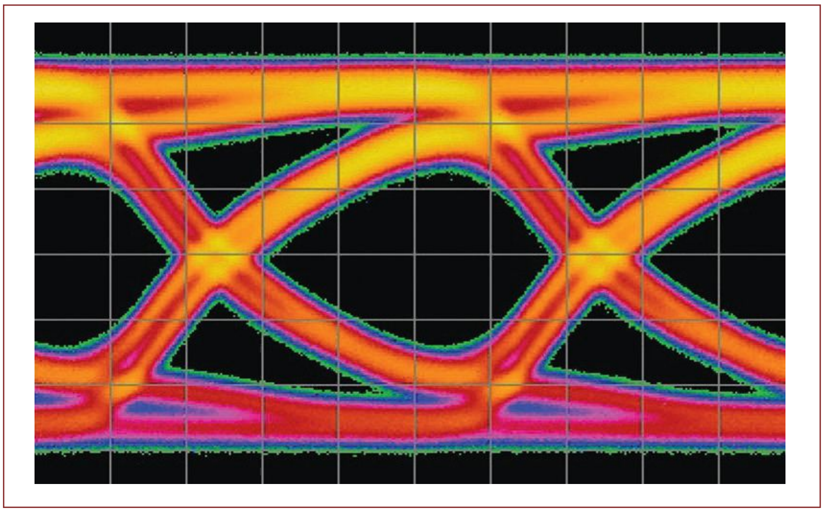

Figure 2 | Eye pattern of a measured signal

Jitter can be segregated into its components, as Figure 3 illustrates. All the components have different origins and show distinct but different probability density functions. This is worth mentioning as the statistical analysis of the eye pattern exploits these properties, by estimating the parameters for the probability density function and then extrapolating these in order to estimate the BER based on the statistical properties of the eye
methods based on error probability (see Figure 1) but in two dimensions (time/magnitude).

- Data Dependent Jitter – is caused by the ISI (intersymbol interference) of the channel
- Bounced Uncorrelated Jitter – is caused by crosstalk from adjacent channels
- Periodic Jitter – caused by undesired modulation like spread spectrum clocking
- Gaussian Jitter – caused by device effects through thermal of shot noise.

The methods described bridge essentially the hardware specific design parameters (layout, material, connectors) to the system relevant parameters, in particular the BER.

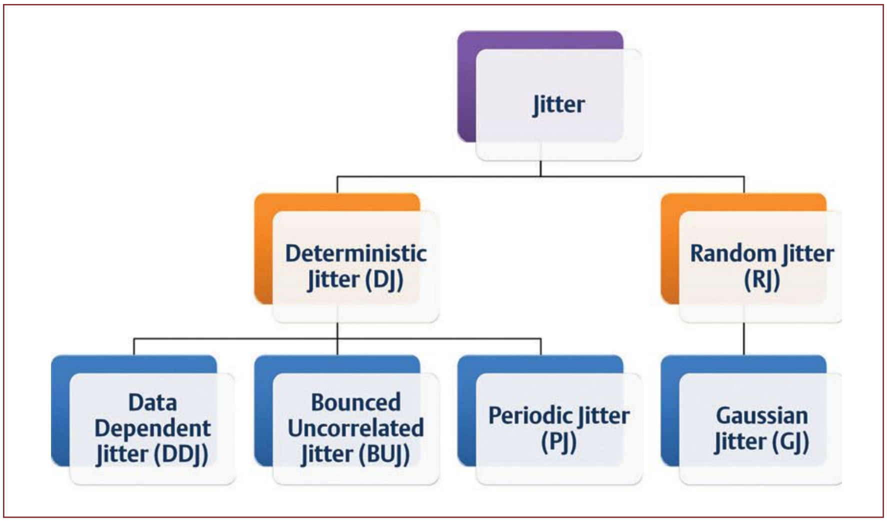

Figure 3 | Jitter classification

System design

Solving the challenge of error-free transmission of a bit from transmitter to the receiver over the transmission channel in the system design is an important topic, but the solution will not automatically guarantee a working system with 40 Gbps data rate to payload slots.

Content delivery

The application scenarios for bandwidth demand beyond 40 Gbps are I/O intensive rather than compute intensive.

If the traffic sources are inside the system or closely controlled by the system, methods defined by the IEEE can be applied to handle the traffic. There are in particular the IEEE 802.1Qbb, IEEE 802.1Qaz, IEEE 802.1Qau, and IEEE 802.1AB that enable Data Center Bridging. Applying these methods, the system resources are managed, and the data sources will not overload the hub switches as well as the individual receiving sink (payload blade).

For traffic from external sources the method just described is no longer feasible. And if for commercial reasons an oversubscription is desired, and the traffic exceeds the forwarding capability of a single blade, modern switches have the ability to statistically distribute the traffic while maintaining a flow granularity up to layer four.

Under the assumption that the bandwidth of a single flow compared to the link bandwidth is small and conversely there are a huge number of flows, switches can utilize the statistic property of the flow distribution. This way the traffic to a payload slot is reduced below the physical limit of the slot bandwidth, maintaining flow affinity to a payload slot.

Level	Simulation performance	Input	Output
Link	High	algorithmic driver models, s-parameter, RLC elements, cross-talk modeling	BER, Jitter, voltage waveforms rise/fall time, magnitude, over shoot
Circuit	Mid	s-parameter, semiconductor devices, RLC elements, distributed transmission lines	Jitter, voltage waveforms rise/fall time, magnitude, overshoot
Field	Low	3D geometric shapes, material parameters	s-parameter for n-port elements, electromagnetic field distribution

Table 1 | Levels of simulation

Tuning the elements

Most of the payload blades in AdvancedTCA systems are compute blades with CPUs of x86 architectures. Applying higher data rates to blades of this type creates scalability issues. For traditional AdvancedTCA bladed architectures such as a symmetrical multiprocessing (SMP) multicore architecture with two CPUs and a 10 Gbps Network Interface Controller (NIC), it is already difficult to achieve this data rate, and substantial effort is necessary to meet this throughput for real-world applications based on the described hardware with a conventional OS: A number of elements need to be tuned.

Achieving the best performance means using modern NIC device hardware features. Integrating the multi-queue features supported by the devices and PCI Express can lead to improvements including:

- Taskset affinity and IRQ affinity
- Multi-queue support
- Direct Cache Access
- RX Check Sum Generation and TX Check Sum Check
- Large Receive/Segmentation Offload
- PCI-SIG SR-IOV

It doesn't matter whether the system runs in SMP, Non Uniform Memory Access (NUMA), or a set of hypervised Virtual Machines (VMs). The applicability is given in any case.

Conclusion

As noted earlier, when the topic is implementing 40 Gbps systems with AdvancedTCA, we cannot take an "auto pilot" approach based on traditional system implementations running at 10 Gbps or below.

And looking to the future we have to ask whether systems will be prepared for the next tier of AdvancedTCA evolution, which is most likely 100 Gbps. Today any answer is quite speculative, and it is important to understand the options:

One option is to improve the channel characteristic using better PCB material and connectors, the second option is optical transmission, and the third option is abandoning the base band modulation and choosing a different modulation scheme.

The first two options are sustainable from a cost perspective. The last one will add much more cost on the silicon component side. Approaches have been reported and seem to be promising. Under this assumption it is possible to say, "Yes! AdvancedTCA is also future proof."

***Dr. Mathias Hellwig** is a system architect, focused on the definition of AdvancedTCA products for the Embedded Computing business of Emerson Network Power. He is a regular contributor to standards committees with bodies such as PICMG and SCOPE. He has previously held a variety of engineering and product management roles with Intel, Force Computers, Infineon, Siemens, and Hewlett-Packard. Dr. Hellwig holds numerous patents in the area of telecommunications and circuit design and received his Masters and Doctorate qualifications from the Ruhr-Universität Bochum in Germany.*

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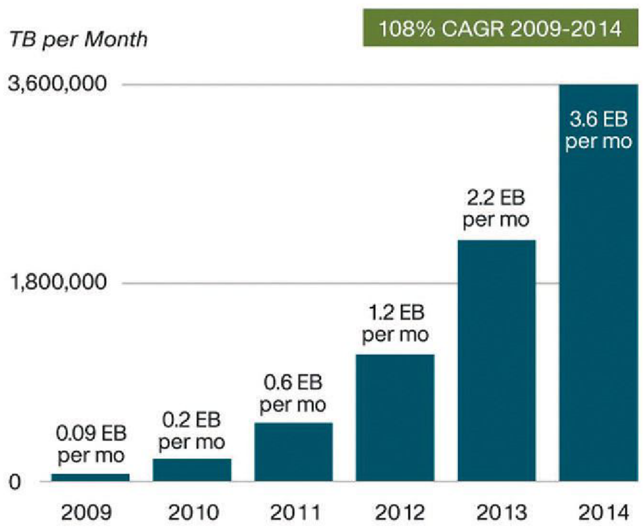
FEATURE

How multicore packet processing software enables cost-effective equipment for 4G networks

By Charlie Ashton

Charlie discusses how specialized software, designed for high-performance processing of network packets and optimized for multicore processors, enables system designers to meet the conflicting goals of high traffic rates, low system power, and minimum system cost.

As advanced services proliferate and video consumes an ever-increasing share of wireless network capacity, the requirements for high-performance processing of network traffic will continue to grow dramatically (Figure 1). Each piece of equipment in the network must achieve higher levels of packet processing performance. At the same time, the equipment must be designed to meet challenging power, cost, and schedule requirements.



Source: Cisco VNI Mobile, 2010

Figure 1 | Total traffic in the core network is growing.

The performance challenge for 4G networks

Designers of 4G telecom infrastructure products, whether LTE or WiMAX, face challenging performance requirements that cannot be addressed with the same techniques that worked for 2G and 3G equipment.

Driven by high-bandwidth Internet applications, the total traffic in the core network is growing at over 100 percent per year, so service providers expect individual network elements such as packet gateways to increase bandwidth by at least a corresponding amount.

At the same time, telecom equipment is increasingly deployed in commercial and outdoor environments without forced-air cooling, placing severe restrictions on the number of high-performance processor subsystems that can be used.

Finally, equipment suppliers operate under ever more challenging cost constraints. Such restrictions apply to both CAPEX and OPEX. Low product cost is essential to support worldwide deployments of 4G networks. At the same time the operating expense of electrical power, both to run the equipment and for cooling, is a major contributor to the calculation of overall Total Cost of Ownership (TCO).

To be successful, developers of 4G networking equipment must deliver solutions that achieve maximum throughput for tomorrow's network traffic patterns (dominated by video and data), while minimizing system-level power consumption and cost.

Packet processing is the key

For 4G networks, 3GPP has specified a flat IP-based network architecture, System Architecture Evolution (SAE), aimed at efficiently supporting massive IP service use (Figure 2). As a consequence, the network architecture is much simpler than existing architectures such as 3G. However, as data, voice, and video all use IP packets, processing these packets efficiently becomes critical to ensure LTE system performance.

On top of the IPv4 and IPv6 protocols that the SAE architecture supports a large number of protocols have to be implemented:

- Low-level protocols such as Internet Protocol Security (IPsec), Robust Header Compression (ROHC) and Virtual LAN (VLAN).
- Within an overall 4G network, a number of protocols support communication between individual subsystems. For example, GPRS Tunneling Protocol (GTP) carries user data via IP tunnels between a Signaling Gateway (SGW) and a base station (eNodeB). Similarly, Stream Control Transmission Protocol (SCTP) implements signaling between the Mobility Management Entity (MME), the SGW, and the eNodeB. Likewise, Generic Routing Encapsulation (GRE) provides VPN connections from the SGW to the Packet Gateway (PGW). And many more protocols are used throughout the network.
- Differentiating the services is also critical. IP QoS is required to give priorities to real-time traffic against pure data traffic. More packet inspection implements the mechanisms to identify the user traffic to better serve users and/or applications.

All these protocols are encapsulated in IP packets. Starting from layer 2 protocols, packet processing software has to analyze successive encapsulated headers as fast as possible.

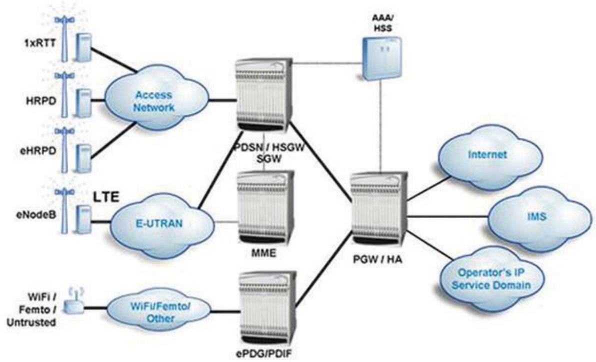


Figure 2 | Processing packets efficiently is key to LTE system performance.

The critical performance challenge for 4G networking equipment is to process these IP packets at the highest possible throughput. In general, the designer's objective is to perform this processing fast enough so that the throughput of the equipment is limited, not by the packet processing performance, but by the speed of the physical network connection, typically 10 Gbps, 40 Gbps or, soon, 100 Gbps. If the processing throughput matches the speed of the network, the system is said to be performing at "wire-speed," maximizing the efficiency of the equipment.

Multicore processors deliver the raw performance

Over the past few years, developers of high-end processors migrated to multicore architectures in order to meet never-ending needs for increased performance. Power is proportional to the square of the clock frequency, thus the traditional processor design approach of continually increasing clock frequencies to boost performance led to prohibitive processor power consumption. The industry adopted multicore architectures in which the cores run at a clock frequency that leads to manageable power consumption for the processor as a whole.

Today, all processors used in high-performance networking products are based on multicore architectures. These platforms provide the ideal environment for implementing the high-performance packet processing that 4G equipment requires.

The Operating System bottleneck

For developers of networking equipment, selecting a multicore processor for their system is only one step in designing a high-performance system solution. Generally, the more complex question is how to architect the software which, as explained above, typically needs to process packets from multiple streams of network traffic at wire-speed.

A standard networking stack uses Operating System (OS) services and falls prey to significant overheads associated with functions such as preemptions, threads, timers, and locking. Each packet passing through the system faces these processing overheads, resulting in a major performance penalty for overall throughput. Furthermore, although some improvements can be made to an OS stack to support multicore architectures, performance fails to scale linearly over multiple cores and a processor with, for example, eight cores may not process packets significantly faster than one with two cores. All in all, a standard operating system stack does a poor job of exploiting the potential packet processing performance of a multicore processor.

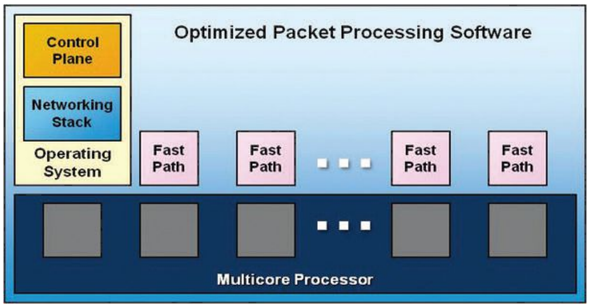


Figure 3 | **Devoting cores to running the fast path maximizes overall system throughput.**

For developers of networking equipment, selecting a multicore processor for their system is only one step in designing a high-performance system solution.

The fast path solution

Specialized packet processing software optimized for multicore architectures can do a better job of taking advantage of multicore packet processing performance (Figure 3). In a well-designed implementation, the networking stack is split into two layers. The lower layer, typically called the *fast path*, processes the majority of incoming packets outside the OS environment and without incurring any of the OS overheads that degrade overall performance. Only those rare packets that require complex processing are forwarded to the OS networking stack, which performs the necessary management, signaling, and control functions.

A multicore processor is well-suited to implementing this kind of software architecture. Most of the cores can be dedicated to running the fast path, in order to maximize the overall throughput of the system, while only one core is required to run the operating system, the OS networking stack, and the application's control plane.

In practice, the designer will analyze the specific performance requirements for the various software elements in the system (applications, control plane, networking stack, and fast path), deciding on the most appropriate allocation of cores to balance the overall system workload. The only restriction when configuring the platform is dealing with the cores that, by virtue of running the fast path are therefore running outside the OS. These cores must be dedicated exclusively to the fast path and not shared with other software. The system can also be reconfigured dynamically as traffic patterns change.

Splitting the networking stack in this way has no impact on the functionality of application software, which interfaces to the same OS networking stack as previously. Existing applications do not need to be rewritten or recertified, but they run significantly faster because the underlying packet processing is accelerated through the fast path environment.

7x – 10x performance improvement

In a typical 4G application such as a PGW or SGW, when the standard OS networking stacks are replaced by optimized packet processing software based on the fast path concept, the networking performance of the processor subsystems will typically increase by seven to 10 times. As Figure 4 illustrates, this massive increase in performance means the system will be able to manage seven to 10 times more users with the same hardware.

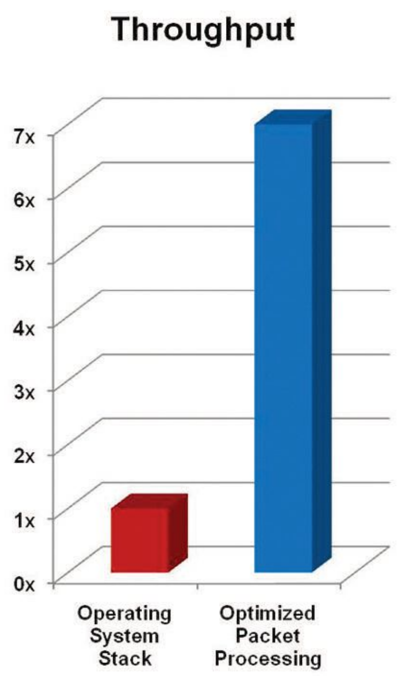


Figure 4 | Designers using fast path implementation can achieve system throughput not possible with a single multicore processor when using a standard OS stack.

Fast path implementation can allow the designer to meet system throughput goals that may have been unachievable on a single multicore processor when using a standard OS stack.

For example, 6WIND has recently demonstrated 10 Gbps Ethernet IP forwarding performance using the 6WINDGate packet processing software running on a 2.40 GHz Intel Xeon processor E5645. In this case, only two of the processor's six cores were required to achieve wire-speed performance, leaving the remaining cores available either for processing more complex fast path protocols or for use by control plane protocols running under the OS.

Energy efficiency and cost reduction

For the network equipment provider, these compelling break-throughs in system performance translate directly into improve-ments in energy efficiency and cost.

In a typical telecom infrastructure product, 60 percent of the power is consumed by processor subsystems (including memory), while the remaining 40 percent comes from I/O, system management, and power supply subsystems. If we assume, conservatively, that

Fast path implementation can allow the designer to meet system throughput goals that may have been unachievable on a single multicore processor when using a standard OS stack.

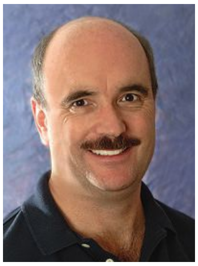
moving to the fast path software architecture described above yielded a 7x performance improvement, the designer can now achieve the same level of system performance using one-seventh the number of processor subsystems. This is equivalent to remov-ing the need for 51 percent of the system's power consumption (given the total consumption of the processor subsystems was 60 percent of the system power). At the same time, the power supply requirements are also reduced. If we assume that saves another 4 percent of the original system power (again, keeping the numbers simple), the total system power consumption has been reduced by 55 percent while retaining the original level of performance.

Looking at this another way, the performance-per-watt or energy efficiency of the system has more than doubled, purely as a result of improvements in the system software.

A similar analysis applies to the system cost. With 50 percent of the overall cost of a 4G gateway typically coming from the processor subsystems, a (conservative) 7x reduction in the number of those subsystems, together with reduced requirements for the system power supply and management features, can enable designers to achieve around a 50 percent reduction in overall system cost through moving to the optimized software solution.

Conclusion

A fast path implementation of the critical protocols avoids the performance bottlenecks imposed by standard operating system stacks. Such an implementation can improve system performance as well as increasing energy efficiency and lowering product cost. For network equipment providers, these benefits represent major sustainable business advantages as they address the challenges of 4G deployments.



Charlie Ashton *is VP Marketing at 6WIND. He is responsible for 6WIND's global marketing initiatives. He also manages 6WIND's partnerships worldwide with semiconductor companies, subsystem providers and embedded software companies. Charlie has extensive experience in the embedded systems industry, with his career including leadership roles in both engineering and marketing at software, semiconductor, and systems companies. He led the introduction of new products and the development of new business at Green Hills Software, Timesys, Motorola (now Freescale), AMCC, AMD, and Dell.*

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FEATURE

Demand for open source service availability solutions elevates

By John Fryer

John draws on his role as Service Availability Forum president to outline the reasons service availability is attracting a growing number of players and cites a real world 4G challenge involving an AdvancedTCA system and a 5-nines uptime demand.

Market demand for service availability has been growing behind the scenes for more than a decade. In the past, service availability solutions were often based on proprietary technologies, developed in-house for specific applications in telecommunications and other industries. However, recent marketplace activities indicate an increasing adoption of standards-based service availability solutions in next-generation networks.

Service availability implies a service is always available. The key principles of service availability extend beyond reactions to a failure to encompass the idea of system monitoring with preventative action being taken before a critical situation occurs. For example, with a memory leak, applications may not correctly release memory segments back to a pool over a long period of time. Despite correct system design and extensive testing, today's complex systems often interact in ways not anticipated by system designers.

Today, we rely on computer-based services for daily activities, such as smartphones for business and personal communication, online financial management and web-based applications and services. While there are complex technical requirements to make these services work, we assume they will be available when needed. When these services become unavailable, there can be a direct impact to consumers. For example, consider a recent outage experienced by Yahoo. The outage came as a surprise as Yahoo is "never" down; however, even a brief outage over the course of an afternoon affected large numbers of users and generated a negative news cycle.

The Service Availability Forum (SA Forum) is an organization enabling the creation and deployment of highly available, mission-critical services by promoting the development of an ecosystem and publishing a comprehensive set of open specifications.

The high-level reference architecture depicted in Figure 1 shows two key sets of SA Forum Application Programming Interface (API) specifications – the Hardware Platform Interface (HPI) specification and the Application Interface Specification (AIS).

The ability to discover, monitor, control, and manage hardware resources in the underlying platform in a manner that is hardware independent comes about through implementation of HPI-specified services. This results in the portability of the HPI-compliant service availability middleware across different hardware platforms that provide HPI services. In the absence of HPI, system designers would have to develop specific support software for every unique hardware platform that needs to be integrated into the system. The engineering effort required to integrate different platforms can quickly become overwhelming, as more platforms need to be brought into the system, and HPI solves this issue.

As long as the hardware platform provides the services specified by the HPI, an HPI-aware user application – the SA middleware in this case – can easily integrate with the underlying platforms without having to make any platform-specific changes. This significantly simplifies the task of platform integration.

The real focus of differentiation in today's market is at the application layer. Just looking at the explosion of applications around mobile devices and web services indicates where the money is to be made. In complex system and network environments, developers must rapidly bring new applications up to speed and combine them in new and different ways. And increasingly, engineers must incorporate service availability characteristics into these applications so that they are "always on."

By authoring applications and services that use the AIS, developers can ensure portability of these applications and services across multiple underlying middleware implementations from different vendors and sources. Finally, the management capabilities specified by the HPI and AIS allow for a unified platform and software management. The AIS from the SA Forum addresses this need with a comprehensive set of services and frameworks, which enable application developers to

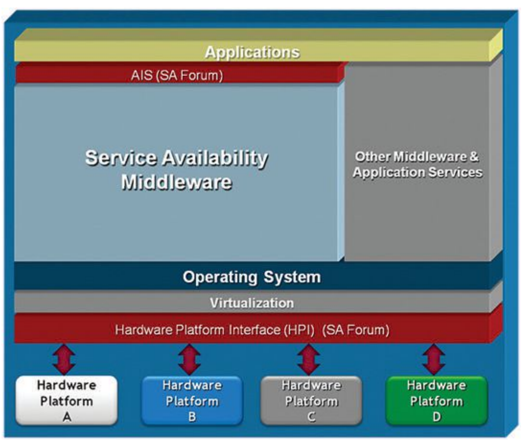

Figure 1 | SA Forum reference architecture

create service available applications in a common, standardized manner. Now an application can be developed once and easily ported to multiple platforms, depending on the deployment requirements. With applications using the same service availability framework, integrating multiple applications together on a common platform becomes a much simpler task. This is why major telecom equipment manufacturers, such as Ericsson, and others are adopting implementations of the SA Forum AIS – to streamline development, accelerate time to market, and reduce costs.

The AIS services are broken down into four main areas, as shown in Figure 2. The AIS platform services provide basic functionality found in many high availability solutions and databases and clustering, but they also include a platform management service for smooth integration between hardware, HPI layer, and the applications. The utility services, as the name suggests, are a set of basic services necessary to accomplish service availability, such as checkpointing – ensuring data is replicated between a live entity and a backup. The management services' standard mechanisms model objects in a system and their relationships. Standard mechanisms also send and receive notification of events and log information on the operation of the system. The AIS can manage the availability of a system through the Availability Management Framework, and includes a Software Availability Framework for creating campaigns to upgrade/downgrade software in a seamless manner. These two key frameworks are, of course, closely related, and form flexible, standard models to describe system actions in the event of a failure or the requirement to manage software changes.

Systems requiring true service availability, such as those in the telecom or networking space and mission-critical systems in aerospace and defense, will use most, if not all, of these services. However, there are many applications which do not require a full implementation of the AIS, yet can take advantage of a subset of the services and frameworks specified.

For nearly a decade, the SA Forum has developed open specifications for service availability middleware, enabling systems to achieve *5-nines* (99.999%) uptime and reduce both planned and unplanned downtime. Benefits of SA Forum's specifications, including enabling an application development ecosystem, reducing cost and risk, and accelerating time to market, are being recognized as the specifications move from development to deployment.

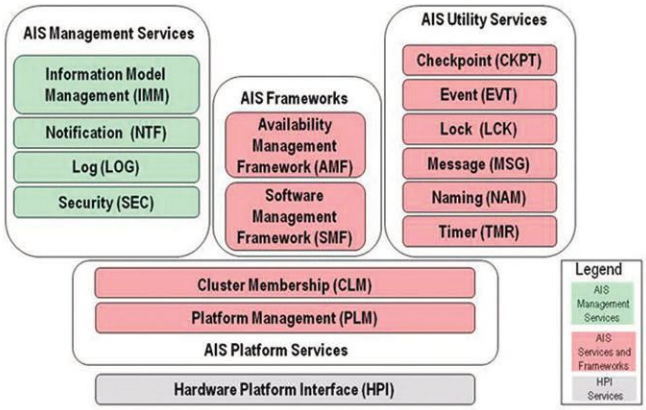

Figure 2 | SA Forum AIS services

Real-world application: 4G wireless broadband controller

One real-world application of the SA Forum specifications includes a 4G wireless broadband controller. The customer's challenge was to build an AdvancedTCA system that would host a wireless broadband access controller application. It had to support one million subscribers with carrier-grade (99.999%) service availability and meet a very aggressive time-to-market goal. The customer wanted to transition from its proprietary middleware solution, which was non-differentiating, and utilize a standards-based solution with newer SA Forum features.

SA Forum member Emerson Network Power provided a turnkey, pre-integrated and pre-validated platform to the customer. The platform included AdvancedTCA hardware, an operating system, and a software suite that implements the SA Forum HPI and AIS services for high availability system and platform management. As a result, the customer gained immediate near-term benefits. The customer deployed in fewer than 18 months – this same deployment would have taken 36 months if the customer had tried to implement its own SA Forum software stack. The solution has been deployed in the field for many years. Additionally, encouraged by the success of the pilot program using an SA Forum standards-based platform, the customer has now moved other projects onto the SA Forum-based platform, which had been adopted for the initial project. The customer is continuously evolving toward standardizing this platform as the common platform for all of its future high availability application needs.

Another trend we are recognizing, along with commercial support from vendors, is robust open source implementation of the SA Forum specifications. For example, the OpenHPI project, which implements the SA Forum's HPI, has an active development community and has been widely deployed through its inclusion in multiple Linux OS distributions. Another example is the Open Service Availability Framework (OpenSAF), an open source implementation of service availability middleware based on the SA Forum specifications. OpenSAF launched in January 2008, with a dedicated development community, multiple major releases, and thousands of downloads of its code.

Move into mission-critical deployments

In 2010, the SA Forum witnessed several events that reflect acceleration of service availability solutions in the market. The first was a public statement by a major equipment manufacturer on commercial adoption and deployment of SA Forum specifications when the OpenSAF Foundation announced Ericsson's deployment of OpenSAF technology in carrier networks. One month after that announcement, SA Forum member company GoAhead Software publically announced its shift to an open source business model and commercial support of OpenSAF with the acquisition of the Aventellis Product Line from Emerson Network Power. These events demonstrate that SA Forum implementations are moving into mission-critical deployments with commercial support available in the market.

One of the keys to success of new open source solutions is to demonstrate adoption and deployment in real environments. This can be a challenge, as companies are often reluctant to publicize their technology choices. This is why the public announcement of Ericsson's deployment of OpenSAF earlier this year is such a significant event, demonstrating that SA Forum specifications can solve Ericsson's service availability requirements, while showing confidence that OpenSAF is a robust solution.

Over the years, we have seen a growing presence of open source technologies in very demanding environments. One primary example is the Linux Operating System, which has a strong development community and is being widely deployed across telecommunications, enterprise, and other markets. A key factor in Linux's growing adoption is the availability of commercial support from companies like Red Hat, Novell, and Wind River. Another key example is the success of Java, with several open source implementations available, such as the GlassFish and JBoss application servers.

The use of open source, standards-based technology has broad appeal and offers commercial benefits. With a dynamic marketplace that includes acquisitions and technology shifts, standards-based solutions allow for increased interoperability and portability, while open source implementations help prevent vendor lock-in and single-supplier risks. Another benefit of using open source solutions is the ability of a company to directly influence and contribute to the technology. For a fraction of the cost to develop the full solution in-house, a company can invest modestly to contribute to open source technologies in areas that directly benefit its business goals.

Another success factor in adoption of open source solutions is the presence of commercial support. The nature of open source allows customers to directly support themselves, and there is a segment of customers who choose this route. For example, an estimated 50 percent of all Linux deployments are self-supported, while the other 50 percent go through commercial vendors like Red Hat. Commercial support of open source solutions is often a requirement and demonstrates the business viability of the technology. The choice of whether to adopt open source directly, along with a self-supported and resourced model, or adopt a commercial distribution of open source is ultimately more of a business decision than a technical one. In the case of SA Forum middleware, the announcement of GoAhead Software as a provider of OpenSAF support is another important step in increasing the deployments of SA Forum technologies. Recently, Ericsson has announced that they have adopted GoAhead's commercial distribution of OpenSAF, a clear indication that they believe a commercial distribution is more cost effective than direct use and support of OpenSAF.

To realize a key goal of helping accelerate the COTS ecosystem, the SA Forum is collaborating closely with other related technology organizations that are also working toward the goal of advancing the ecosystem of open source service availability solutions.

The SA Forum will continue its focus on making its specifications even more accessible by providing new educational resources on developing highly available applications using SA Forum-based middleware. For more information, please visit http://saforum.org.

John Fryer *is President of the Service Availability Forum. He is also the Vice President of Business Development for GoAhead Software. John has more than 25 years of experience in the communications industry in a variety of marketing and engineering positions. John holds a B.Sc. with Honors in mathematics from the University of Nottingham, England. H e can be contacted at admin@saforum.org.*

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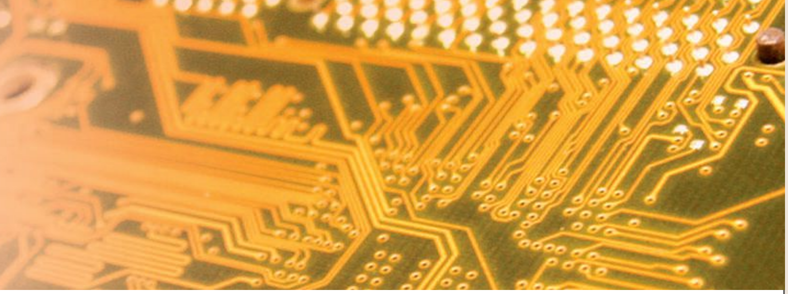

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Breakthrough channel density & features for TCM to IP conversion of signaling and/or media traffic • 4 channelized OC-3/STM-1 links or 1 channelized OC-12/STM-4 link • 622MB/s aggregate transmission rates • 8,064 DS0 time slots • 2,048 channels of HDLC encapsulation for embedded DS0 or subrate data links • 4 Gigabit Ethernet links • telecom clock management • FPGA with integrated PowerPC control • Interworking software enables HDLC to IP for Frame Relay, SS7, LAPD & more • 2-way Automatic Protection Switching (APS) • Flexible, efficient & cost-effective for 3G RNC, SGSN, Router/Multi-Service Switch, BSC, Media/Voice Gateway, Edge Aggregation

http://www.iphase.com/products/product.cfm/AMC/395 **advancedtca-systems.com/p30105**

Interphase Corporation — iSPAN 36701 4G Wireless Base Station AMC

Application-ready eNodeB Base Station AMC + pre-integrated LTE software Layers 1-3 and iWARE APIs for fast-start development – ideal for new 4G Compact Base Stations • All-in-1 baseband/control/network functions • Powerful Mindspeed™ Transcede™ Family System on a Chip (SoC) multicore processor • Three 10 MHz sectors 2x2 in one device or three 20 MHz sectors with 2x2 Tx/Rx in one device • Backhaul and air interface security • Optional onboard GPS Receiver & Precision clock sourcing for mobile deployment • Modular/scalable • Supports femto-, pico-, micro-, & macrocells • Use for standalone eNodeB or complete LTE/EPC network • See whitepaper at www.iphase.com/LTE

http://www.iphase.com/products/product.cfm/AMC/459 **advancedtca-systems.com/p44403**

Kontron — AM4020 High Performance AMC

The AM4020 is a powerful single-width processor module, which is designed around the new Intel® Mobile Core™ i7 processor. With up to dual 2.53 GHz, the AMC module offers the ultimate in computing power and integrated graphics when utilized in MicroTCA™ and AdvancedTCA® integrated platforms. The single-width module integrates the memory controller, PCI Express and the graphics processor within the multi-core processor.

www.kontron.com **advancedtca-systems.com/p46584**

Kontron — AM4211 Packet Processor AMC Module

The AM4211 Packet Processor AMC module is designed with the Cavium Networks OCTEON® II CN6335 cnMIPS64® II 6-core processor, helping to accelerate system designs for 4G, LTE, WiMAX base station vendors. Platform design considerations for the Kontron AM4211 include using it as an eNodeB and LTE network element component or, in combination with full-scale AdvancedTCA® blades, as a co-processor Network Interface Card (NIC). The Kontron AM4211 supports 1x 10GbE to the front and is interoperable with third-party DSP AMCs. Also supported is the IEEE 1588 timestamp for Ethernet time synchronization.

www.kontron.com **advancedtca-systems.com/p46581**

Kontron — **AM4530 NAS Storage AMC Module**

Unique in the market, the Kontron AM453x AMC module is a cost-competitive storage solution for MicroTCA and ATCA platforms that require Network Attached Storage connectivity. Specifically for MicroTCA-based systems, the AM453x module provides access to storage for Processor AMC modules that are without a SATA connection. From an ATCA platform standpoint, the AM453x can be a single point of code storage for the entire system when populated in one or both AMC slots of the Kontron AT89xx switch. This makes it an ideal solution for fast boot code or application code updates.

www.kontron.com **advancedtca-systems.com/p46582**

N.A.T. GmbH — **NAMC-ECAT**

EtherCAT slave module in AMC (Advanced Mezzanine Card) form factor • Single compact, mid or full size module • PICMG AMC.0 R2.0 • Backplane Interface: PCIe 1 lane to Port 4 • PICMG AMC.1 R1.0 • IPMI and Compliance: PICMG AMC.0 R2.0 • EtherCAT System Controller: ESC ET1100 EtherCAT-ASIC 3 RJ-45 at front panel • Memory: 8 kByte • Indicator LEDs: 1 blue LED; 2 status LEDs; 6 link status LEDs • Host Operating System Support: OK-1, Linux; VxWorks (on request) • Power Consumption: 3.3V MP 0.1A (max.) 12V 0.3 A (typ.) • Environmental: Temperature (operating): 0 °C to +60 °C with forced air cooling, Temperature (storage): -40 °C to +85 °C • Relative Humidity: 10% to 90% at +55 °C (non-condensing)

www.nateurope.com **advancedtca-systems.com/p46085**

Pinnacle Data Systems, Inc. — **AMC-E24D Dual Display Graphics+Storage**

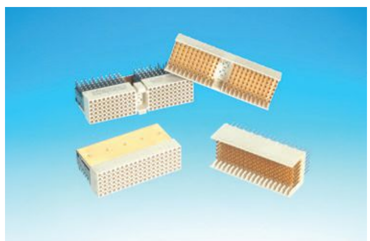
This mid-size AMC offers both high-performance dual display graphics and SATA onboard storage in a single module. Featuring the AMD Radeon™ E2400 graphics controller, the AMC-E24D module supports two independent high-resolution display devices (one digital HDMI and one analog VGA) and features 128MB of on-chip GDDR3 video memory for fast, high quality 2D and 3D graphics rendering. In addition, the module adds enterprise-grade SATA storage to xTCA systems. It carries a 2.5 inch hard drive (HDD) or solid state drive (SSD) with up to 320GB capacity for convenient local boot-up and storage.

info.sales@pinnacle.com **advancedtca-systems.com/p45801**

Hypertronics — **cPCI 2mm**

Immune to shock and vibration fretting • High-temp LCP insulator meets NASA outgassing requirements • Reverse gender to commercial 2mm products • Shield prevents EMI/RFI • Configured on a 2mm center-line with six rows • Uses 0.4mm Hypertac contacts that feature less than eight milliohms of contact resistance and a current rating of 1.0A • Modular in design, the connector is variable in length and can be changed in increments of five contacts

www.hypertronics.com **advancedtca-systems.com/p43694**



Positronic Industries — **Environmental D-subminiature**

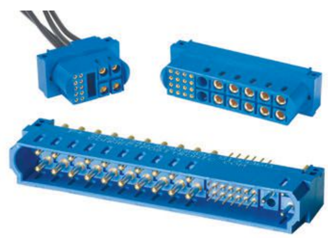
Environmental D-subminiature connectors are available in standard density options with 9, 15, 25, 37 and 50 contacts • High density options are available with 15, 26, 44, 63, and 78 contacts • Contact termination options include solder cup, straight and right angle printed board mount and pre-wired assemblies • A wide variety of options and accessories is available • Most contact variations are offered with Positronic "Unibody" connector insert design • This unique design yields improved temperature range, increased performance and lower cost • For more information and to receive your free catalog, visit www.connectpositronic.com/products/61/EnvironmentallySealed/

www.connectpositronic.com **advancedtca-systems.com/p46572**

Positronic Industries — **Scorpion Connector**

The best connector to fit your needs is the one you design yourself • The Scorpion connector can be configured for use as a power connector, a signal connector, or a combination • Modular tooling, which provides one-piece insulator, allows for quick turnaround of an almost infinite variety of customer-specified contact variants • Customers can configure a power connector for their individual requirements from a wide array of "modules" • Power options include 60 amperes size 8, 40 amperes size 12, and 30 amperes size 16 contacts, with contact resistance values as low as 0.001 ohms • Size 22 signal contacts are also available

www.connectpositronic.com **advancedtca-systems.com/p43057**



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American ELTEC Inc.
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Adax, Inc. **PacketRunner**

The Adax PacketRunner (APR) is an intelligent ATCA carrier blade designed for process-intensive telecom applications. The on-board Cavium OCTEON 5650 multi-core processor, memory, and cache give developers a high-performance, highly flexible and scalable blade for LTE, 4G, IMS, and Next Generation Mobile telecom networks. The APR delivers the perfect ATCA subsystem for user and control plane applications.

Features

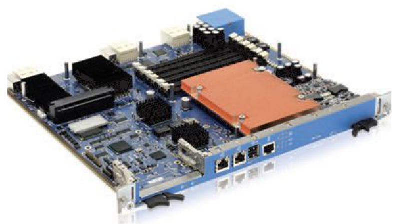
- Cavium OCTEON Plus CN5650, 12 cores at 750MHz
- 4 AMC bays for Adax and/or 3rd party AMC cards
- 2 GB of DDR2 Memory (options for 4 GB and 8 GB DDR2 memory)
- Robust power & thermal management
- Ethernet Switch with: 2x 10 GbE to the system Fabric domain – 2x 1 GbE to the system Base domain – 10 GbE from Cavium to Ethernet switch – 16x GbE, 4x 1GbE to each AMC bay ATCA subsystems

www.adax.com **advancedtca-systems.com/p46548**

adax Foundations for the ALL-IP Network TELECOM SPECIALISTS 25+ YEARS SINCE 1982

Kontron **AT8050 10GbE 6-Core IA Processor Blade**

The Kontron AT8050 supports two Feature-Rich Processor Options: Single Intel® Xeon® Six-Core 5600 Series and Single Intel® Xeon® Quad-Core 5500 Series. It is optimized for virtualization due largely to the complementary Intel 82599 10 Gigabit Ethernet controller that works to reduce I/O bottlenecks and boost server performance. With an available AdvancedMC slot, wireless/telecom equipment manufacturers can add an assortment of Kontron AMC storage and I/O modules for added functionality. A rear transition module built with an SAS controller is also available.



www.kontron.com **advancedtca-systems.com/p46580**

Pinnacle Data Systems, Inc.

ATCA-F1 Dual Socket AMD Operton Processor Blade (Six-Core CPUs)

PDSi's Dual AMD Opteron™ ATCA® Blade with RTM Interface (ATCA-F1) is a military-proven, high-performance general purpose server platform for AdvancedTCA® systems. Architected around AMD Opteron processors with HyperTransport™ technology, it features two CPU sockets that can be populated with the latest AMD 2419 EE "Embedded Istanbul" 1.8GHz six-core processors, for a total of twelve cores. PDSi's ATCA-F1 blade supports up to 32GB of 667MHz memory.

This third generation blade features a Zone 3 interface for connection to PDSi's ATCA-RT01 rear transition module (RTM), which adds SAS or SSD storage, video, and USB resources. Other on-blade features include a CompactFlash site and an AdvancedMC™ slot for additional I/O or further storage expansion. See PDSi's AMC-E24D module for an excellent space-saving AMC combining SATA storage and dual hi-res video. Customization and ruggedization welcomed!

info.sales@pinnacle.com **advancedtca-systems.com/p46014**

Kontron

CP6002 and CP3002 Processor Boards

Intel Core i7 Processor Boards

The CP3002-RC is conduction cooled and supports operational temperatures ranging from -40 °C to +85 °C according to VITA 47 recommendations. On the memory side, up to 8 GB of soldered DDR3 1066 MHz ECC memory ensures data accuracy for demanding and mission-critical and safety-critical applications.

The CP6002, a CompactPCI PICMG 2.16 compliant 6U CPU board, comes with various rugged levels. Four GbE, six SATA ports, DVI & HDMI, onboard HDD and CompactFlash round out the feature set.

www.kontron.com **advancedtca-systems.com/p46585**

Adax, Inc.

Packet Processing Subsystem Product Set

- **Adax PacketRunner (APR)** – The APR is an intelligent ATCA carrier card for I/O intensive telecom applications. It has 4 AMC slots to take any combination of Adax or other industry standard AMC cards and the on-board Cavium OCTEON processor, memory and cache provide a high performance, highly flexible and scalable blade for IP transport, Carrier Ethernet (CE), QoS, Security, Bandwidth Management, Packet Processing, I-TDM and Signaling applications in NGMN, IMS, and LTE networks.
- **PacketAMC (PktAMC)** – The PktAMC board provides Intelligent Networking, Control Plane, Security, QoS, and Wireless applications, delivering a highly available, high-performance carrier-grade transport from the Edge to Core networks.
- **QuickPort** – Adax Development and Support Suite for the Cavium Processor. Adax has modified and enhanced the standard Cavium SDK to assist in porting your own or 3rd party applications to the APR and PktAMC. QuickPort greatly reduces your development time and cost, providing a fast time to market for your application.

www.adax.com **advancedtca-systems.com/p46549**

Adax, Inc.

PacketAMC

Adax's long experience in signaling reliability and performance is brought to bear on user and control plane applications for the All-IP Network with the PacketAMC (PktAMC). The PktAMC provides front-end intelligent processing for Traffic and Bandwidth Management, QoS and Security on all Wireless applications, delivering a highly available, high-performance, carrier-grade transport from the Edge to Core networks. **Features:** ATCA Subsystem for LTE, 4G, IMS, NGMN, VoLTE, UMA & Femtocell applications • High-performance hardware acceleration with Cavium OCTEON Plus 5645 and 5650

www.adax.com **advancedtca-systems.com/p46815**

Interphase Corporation

iSPAN 36MC2 10 GE OCTEON Packet Processor

Mid-size and Full-size AMC solutions based on Cavium OCTEON Plus (56xx) multicore processors with configurations for 1x or 2x 10 GE SFP+ interfaces • OCTEON Plus 56xx MIPS processors running at up to 600 MHz • 8, 10 or 12 core • AMC.2 Type E2, ports 0, 1 (2x 10 GE)/AMC.2 Type 5E2, ports 0, 1/XAUI ports 8, 9, 10, 11 (1 x 10 GE) • AMC.1 Type 4x4 PCIe lanes on ports 4-7/PCIe 100 MHz clock on AdvancedMC CLK3 • 2 GB DDR2 with option of 4 GB • A pin compatible chip that can support 8 to 12 cnMIPS® plus MIPS 32/64 architecture compatible cores

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Elma — **Conduction & Convection Cooled COTS (ATRs)**

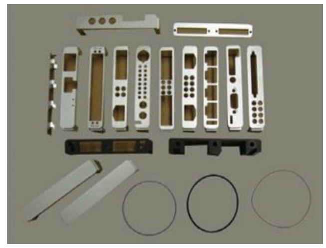
Elma's full line of convection cooled ATR (Air Transport Rack) enclosures offers a standardized, cost-effective solution for CompactPCI, VME, VME64x, VXS, VPX, and MicroTCA based applications • COTS, convection or conduction cooled 1/2, 3/4, 1, or 1 1/2 ATR per ARINC 404A • IEEE 1101.10 compliant • Full range of isolated military power supplies from 150 to 750 watts • VME, VXS, VPX, cPCI, or custom bus formats • Modular design allows for customization with reduced cost and lead time • Capacity for 5, 7, 12, or 15 slots of 3U and 6U boards • Advanced airflow distribution through card cage (convection)

www.elma.com — **advancedtca-systems.com/p46605**

Globalux Industrial Co., Ltd. — **PMC Bezels**

Our PMC bezels both functionally and cosmetically are among the highest quality in the industry • We have made more than 350 custom bezel cut outs in the last three years • Conform to IEEE P1386 • With our engineering expertise and substantial investment we developed a proprietary U-shape groove that fits with choice of stainless steel O-ring or metal impregnated elastomer O-ring, and such combinations are gaining among the top EMC suppression testing results • Cut by high-speed Japanese milling CNC • Choice of aluminum bezels or zinc die cast bezels • Special design tray using silicone free and anti-static material for our PMC bezels packing ensures good protection during transit

www.globaluxind.com — **advancedtca-systems.com/p46823**



Pentair Technical Products, Schroff brand — **AdvancedTCA Systems**

Broadest range of 40GB AdvancedTCA systems, including 2-, 6- and 14-slot • AC and DC options for both NEBS Telco and cost-sensitive enterprise requirements • Backplane topology options, including dual star, full mesh and triple replicated mesh with bused or radial IPMB • Proven high-performance thermal solutions for 300 Watts per slot and beyond • Schroff brand Shelf Management Architecture based on Pigeon Point SHMM-500 technology • Full range of accessory products, including air baffles, front panels, test boards and cabinets • Engineered custom configurations to meet your exact requirements • Find out more: www.a-tca.com and www.schroff.us

www.a-tca.com — **advancedtca-systems.com/p46576**

Pinnacle Data Systems, Inc. — **ComputeNode™ CompactPCI Chassis Products**

PDSi's ComputeNode line offers a range of NEBS Level 3-compliant CompactPCI chassis in sizes from 1U to 4U. These carrier-grade chassis include a horizontal design, superior air cooling, cPCI and cPSB (PICMG 2.16) backplanes, redundant hot-swappable fans, and hot-swappable front accessible AC or dual-feed DC power modules with power filters in most cases. All 2U and larger ComputeNode platforms include PDSi's unique Alert!Node™ (or Enhanced Alert!Node) alarm card, an intelligent chassis management controller for comprehensive fan and power monitoring. The Alert!Node card does not occupy a CompactPCI slot, front or rear.

info.sales@pinnacle.com — **advancedtca-systems.com/p44295**

SIE Computing Solutions, Inc. — **505 CompactPCI**

505 Series 3U 7-slot CompactPCI benchtop chassis is a configurable enclosure for systems in embedded telecommunications, military, and test and measurement applications • Compact and lightweight aluminum system with front and rear slots to allow for a variety of configurations • Designed for thermal reliability across a variety of embedded computing applications with support for AC or DC input and pluggable positive pressure cooling scheme in front • 7-slot 3U CompactPCI backplane, left-justified CPU slot and coding keying for 5V operation • Backplane power-monitoring LEDs for CompactPCI voltages and a rear I/O with AC/DC switch and ESD jack are integrated with NEBS compliance in mind

www.sie-cs.com — **advancedtca-systems.com/p46749**

Southco — **CompactPCI Ejector Handle**

Microswitch protection against short-circuits during modular board hot swapping in network, telecom, and general computing applications • Ergonomically friendly design for easy operation • Ample grip and a straightforward action with low operating force to simplify the user experience

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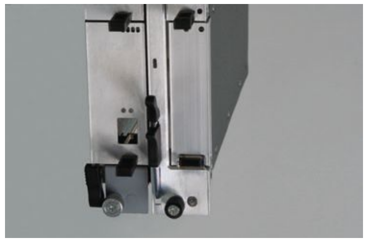
Enclosures

Southco — **Flush Mount AdvancedMC Module Handle**

Microswitch protection against short-circuits during modular board hot swapping in network, telecom, and general computing applications • Minimizes protrusion on the front of the module faceplate • Satisfies all requirements of the PICMG AMC.0 R2.0 standard • Designed to align neatly with the faceplate for better appearance and to prevent potential snagging of cables in use

www.southco.com — **advancedtca-systems.com/p37286**



Vector Electronics & Technology, Inc. — **cPCI, PXI, VME, VXI Custom Packaging Solutions**

VME and VME64x, CompactPCI, or PXI chassis are available in many configurations from 1U to 12U, 2 to 21 slots, with many power options up to 1,200 watts. Dual hot-swap is available in AC or DC versions. We have in-house design, manufacturing capabilities, and in-process controls. All Vector chassis and backplanes are manufactured in the USA and are available with custom modifications and the shortest lead times in the industry. Visit www.vectorelect.com, email inquire@vectorelect.com, or call 1-800-423-5659 to discuss your application.

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MicroTCA

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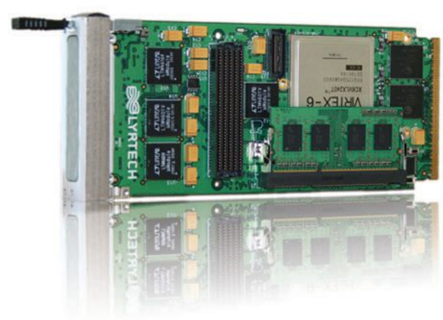
Lyrtech — **Perseus 601X**

The Perseus 601X AMC is designed around the powerful Virtex-6 FPGA, combining unsurpassed fabric flexibility and a colossal external memory, as well as benefiting from multiple high-pin-count, modular add-on FMC-based I/O cards. The Perseus 601X is intended for high-performance, high-bandwidth, low-latency processing applications. The card also takes full advantage of the Virtex-6 FPGA's power, which, when combined with Lyrtech's advanced software development tools, makes it perfect for reducing the size, complexity, risks and costs associated with leading-edge telecommunications, networking, industrial, defense and medical applications. Finally, the Perseus 601X's FMC expansion site (VITA 57.1) offers almost endless I/O possibilities.

www.lyrtech.com — **advancedtca-systems.com/p45729**

LYRTECH



Kontron — **AM5030 and OM6040D**

The Intel® Xeon® Quad Core Processor AMC and the 10G MicroTCA Platform OM6040D are designed for compute-intensive applications. The modular platform is dedicated for applications in the industrial automation, image processing and medical markets, which benefit from the processing power of a high-performance AMC module like the AM5030 and high-speed fabric of 10GbE on the backplane. Filled with four powerful AM5030 processor modules equipped with the next generation Intel® Xeon® processor LC5518, the OM6040D becomes a very compact high-performance platform.

www.kontron.com — **advancedtca-systems.com/p46583**

Storage

Elma Electronic Inc. — **Secure PMCDisk**

For securely erasing and write-protecting sensitive data in harsh environments found in military and defense applications • High-capacity mass data storage mezzanine supports 10 major defense agency secure erasure procedures via a front panel push button with an LED indicator to confirm data erasure • Enables write protection via a front panel toggle switch • Defense agency standards supported: fast clear/initialize; clear; DoD NISPOM 5220.22-M and 5220.22-M-Sup 1; NSA/CSS Manuals 130-2 and 9-12; AR 380-19; NAVSO P-5239-26; AFSSI-5020; and IRIG 106-07 • Use on any board that has an IEEE 1386.1-compliant PMC site, such as cPCI • RoHS-compliant • Ships with a 2.5-in. solid state flash drive

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Adax, Inc. **HDC3-PMC**

The HDC3 is the third generation of the highly successful Adax SS7 controller and offers up to 8 T1, E1 or J1 trunks per card. Specifically designed to meet the demands of wireline, wireless and convergence platforms, the HDC3 excels at traditional TDM SS7, High-Speed ATM SS7 as well as I-TDM voice interworking. The HDC3 provides a high-density, high-performance solution for signaling and interworking applications.

Features

- 8 software selectable trunks of full E1, T1, or J1 per card
- Up to 248 LSL MTP2 links per card with high line utilization
- Support for up to 128 channels of Frame Relay or a combination of 248 channels of HDLC, X.25, LAPB/D/F/V5 protocols
- Support for M3UA, M2PA, SCTP and M2UA
- Supports I-TDM SFP.1, 125uS for PCM to Ethernet voice traffic interworking
- PMC, AMC, PCI and PCIe (Full height and Low-Profile and ExpressModule) board formats

www.adax.com **advancedtca-systems.com/p46551**

Pinnacle Data Systems, Inc. **PMC-SD18 and XMC-SD18 SATA HDD/SDD**

These new SATA Storage Modules are offered in both PMC and XMC formats. Both provide high capacity SATA storage using compact 1.8 inch hard disk (HDD) or solid state drives (SSD) – up to 160GB of storage is available with either drive type. Whether configured with an economical rotating HDD or with a highly shock-resistant SSD, these low profile modules fit comfortably into VITA 42.3-compatible VME, CompactPCI®, AdvancedTCA®, and PCI Express processor boards without risk of mechanical interference.

info.sales@pinnacle.com **advancedtca-systems.com/p45802**

Pinnacle Data Systems, Inc. **XMC-E24D/PMC-E24D Dual-Display Graphics**

PDSi offers these high-performance dual-display graphics modules in both XMC and PMC form factors. Using the ATI Radeon™ E2400 graphics controller from AMD, these modules enable VME, cPCI, and AdvancedTCA systems to take full advantage of AMD's embedded advanced graphics technology. They provide simultaneous independent support of either one digital DVI and one VGA analog display or two VGA displays at 32-bit color and up to 2048 x 1536 resolution.

info.sales@pinnacle.com **advancedtca-systems.com/p46816**

Pinnacle Data Systems, Inc. **AMD Socket S1 COM Express Module**

PDSi's AMD Socket S1 COM Express Module (COMX-S1) is a low-cost, compact, embedded computing core with the capability to drive a broad range of OEM applications. Built around AMD's x86-based Socket S1 processors, it enables 64-bit computing at a progression of performance levels from the ultra-low-power AMD Sempron™ 2100+ (perfect for fanless applications) to the dual-core muscle of the AMD Turion™ X2 TL62. The Computer-On-Module design is fully compliant with PICMG COM Express Type 2 specifications, offering a large variety of interfaces to cover the needs of most embedded applications.

info.sales@pinnacle.com **advancedtca-systems.com/p44294**

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Avionics Interface Technologies — **PXI-C1553-1/2/4**

MIL-STD-1553 Test and Simulation Module for CompactPCI/PXI/PXIe • Dual Redundant, Single, Dual, or Quad Stream configurations • Concurrent Bus Controller, 31 Remote Terminals, and Chronological Bus Monitor • Full Error Injection/Detection • FPGA-based Hardware Architecture • PXI interrupter, star trigger, and clock • Complex Triggering capabilities for Capture/Filtering, 100% Bus Recording • Real-Time Recording and Physical Bus Replay • IRIG-B Time Encoder/Decoder • Flight Simulyzer 1553 Bus Analyzer Software • Flight Director Windows-based Parameter Processing Software

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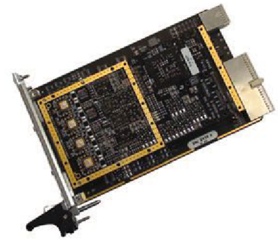

Hartmann Elektronik — **CompactPCI System Platform**

2U Inclusive Voltage & Temperature Monitoring • 6U, 4-slot CompactPCI backplane with rear I/O • CompactPCI power supply 250 W • Hot swap fan drawer with 3x 80 mm fans – also Rear I/O area • Filter, easy switchable without tool • Voltage monitoring • Temperature control • Display if fan is not working • Monitoring of power-in of the fan drawer by green LED on the front • Configuration of the characteristic curve of the fans with DIP switches, to adapt the cooling to the demand • Hartmann Elektronik offers system platforms in different sizes and variants •

www.hartmann-electronic.com — **advancedtca-systems.com/p43778**

WaveTherm Corporation — **cPCI and uTCA.3 SolidWedge wedgelock**

SolidWedge wedgelock solutions

- ~3x thermal contact area over traditional style wedgelocks
- Higher clamping force
- Zero insertion force
- Less galling of mated surfaces / higher number of insertion cycles
- Low profile leaves maximum board space available for critical functionality

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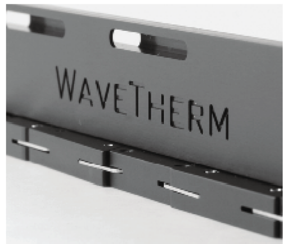

Interface Concept **IC-PQ3-XMCa**

Ultra low power Processor XMC module, based on the Freescale PowerQUICC III MPC8536E processor • Gigahertz-class complex application processing abilities and high-speed connectivity in a small board footprint • Typical consumption in full-operational configuration (1 GHz) is 10 W • Ideally suited for a large range of embedded applications such as compute-intensive solutions requiring high-speed I/O transactions, Gigabit Ethernet interfaces for high-performance network connectivity or redundant failsafe links, powerful control element for network switches, storage subsystems, network appliances, print and imaging devices, etc. • Up to 1 GB DDR2- ECC, 128 MB Flash, 4 GB of NAND Flash, and up to three GbE ports

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Lyrtech **ADAC250**

The ADAC250 FMC is designed around the high-performance A/D and D/A conversion technology from Texas Instruments – it integrates one dual, 14-bit, 250 MSPS A/D converter (ADS62P49) and a dual, 16-bit, 1 GSPS D/A converter (DAC5682Z; also capable of a 2-4× interpolation mode). Combined with multiple clocks and synchronization modes, the ADAC250 is at its best in DSP applications such as software-defined radio, advanced telecommunications (MIMO systems, cognitive radios, beamformers, LTE, WiMAX), signal intelligence (SIGINT), radar, sonar, and medical imaging applications.

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North Atlantic Industries **67C3 OpenVPX Multi-function I/O**

Multiple functions on a single slot 6U OpenVPX card • OpenVPX slot profile: SLT6-BRG-4F1V2T-10.5.1 • User can specify up to six different function modules • Control via VME or Dual Gigabit Ethernet interfaces • sRIO (1x) or PCIe (x1) options • Connections via front panel, rear panel or both • Designed for commercial and rugged applications • Conduction or convection cooled versions

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Pinnacle Data Systems, Inc. **XMC-GBX Quad Gigabit Ethernet Adaptor**

This new quad gigabit Ethernet XMC is a high-performance, low-latency network adaptor providing four high-speed Ethernet interfaces for use with VITA 42.3-compatible VME, PCI Express, CompactPCI®, and AdvancedTCA® processor boards. It is available in three configurations offering a mix of front and rear port access. Wide internal data paths eliminate performance bottlenecks. The parallel and pipelined logic architecture is optimized for Gigabit Ethernet and efficiently handles packets with minimum latency. Using widely accepted Intel 82571EB Ethernet controllers, this adaptor offers up to four 10BASE-T/100BASE-Tx/1000BASE-T copper ports with front-mounted RJ-45 connectors and full status indicators.

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Pentek, Inc. **Cobalt 78630**

1 GHz A/D, 1 GHz D/A and Virtex-6 FPGA – PCI Express Cobalt Board • Complete radar and software radio interface solution • Supports Xilinx Virtex-6 LXT and SXT FPGAs • Includes 1 GHz 12-bit A/D and 1 GHz 16-bit D/A • Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM • Sample clock synchronization to an external system reference • LVPECL clock/sync bus for multiboard synchronization • LVDS connections to the Virtex-6 FPGA for custom I/O • PCI Express (Gen. 1 & 2) interface up to x8 wide • User-configurable gigabit serial interface • Other formats available: 3U and 6U cPCI, PCI, XMC, 3U OpenVPX

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Pentek, Inc. **Cobalt 78650**

Two 500 MHz A/Ds • Digital Upconverter • Two 800 MHz D/As • Virtex-6 FPGA – PCI Express Cobalt Board • Complete radar and software radio interface solution • Supports Xilinx Virtex-6 LXT and SXT FPGAs • Two 500 MHz 12-bit A/Ds • One digital upconverter with two 800 MHz 16-bit D/As • Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM • Sample clock synchronization to an external system reference • LVPECL clock/sync bus for multi-board synchronization • LVDS connections to the Virtex-6 FPGA for custom I/O • PCI Express (Gen. 1 & 2) interface up to x8 wide • User-configurable gigabit serial interface • Other formats available: 3U and 6U cPCI, PCI, XMC, 3U OpenVPX

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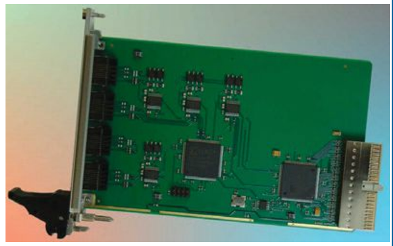

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Adax, Inc. — **HDC3 PCI Express Boards**

The HDC3 is the third generation of the highly successful Adax SS7 controller and offers up to 8 T1, E1 or J1 trunks per card. Specifically designed to meet the demands of wireline, wireless and convergence platforms, the HDC3 excels at traditional TDM SS7, High-Speed ATM SS7 as well as I-TDM voice interworking. The HDC3 provides a high-density, high-performance solution for signaling and interworking applications.

The HDC3 is available in PCI, PCIe, LPe and the new ExpressModule form factors, all of which share a common software driver and have a consistent API for application portability. This makes the HDC3 card a highly flexible, scalable and portable signaling solution for all system architectures that maximizes protection of investment.

www.adax.com **advancedtca-systems.com/p46550**

ALPHI Technology Corporation — **PCI Express Mini – 1553 Controller**

PCI Express x1 lane interface • Dual redundant MIL-STD-1553 interface • DDC Total-ACE Chip • 64K Shared RAM • Programmable bus controller, remote terminal, or bus monitor modes • Multiprotocol Support of MIL-STD1553A/B • Software compatible with all DDC Ace+ Family • On-chip transceivers and Transformer coupled • +3.3V operation and logic • Extended temperature -40 °C to +85 °C

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AMTELCO XDS — **XDS H.100 PCI Express E&M Line Interface Board**

AMTELCO XDS offers several H.100 PCI Express boards, including the E&M Line Interface Board. This board contains eight ports, with each capable of 2-wire, 4-wire, or Radio Interface (Push-to-Talk) operation, supporting type I or type V signaling protocols. Other XDS H.100 PCI Express boards include the 12/24-Port Loop Start Board, the 24-Port Station/DID Board, and the 4/8-Span T1/E1 Board. Software drivers are available for the most common operating systems, including an XDS Channel Driver for Asterisk® environments. Driver packages are distributed free of charge to XDS customers, with open source code for the driver and all supporting applications.

xds.amtelco.com **advancedtca-systems.com/p46558**

Excalibur Systems, Inc. — **4000 Magic Plus PCI Express**

The EXC-4000PCIe (4000 Magic Plus PCI Express) is a x1 PCI Express card complying to PCIe specification 1.1 • Supports up to four independent 4000 family avionics communication modules, allowing multiple different protocols to be mixed and matched on a single card • Supports fast DMA transfers for reducing processor and system latency time • Modules available: MIL-STD-1553, MIL-STD-1760, MMSI, H009, ARINC-429, ARINC-708, Serial, Discrete and CAN bus • Supports extensive error injection and detection capabilities, IRIG B Time Code input • Can be ordered with operating temp range: -40 °C to +85 °C and conformal coating • Supplied with C drivers, incl. source code • Mating connector for I/O connection

www.mil-1553.com **advancedtca-systems.com/p45234**

EUROTECH **A6pci8029 – 6U cPCI with Atom processor**

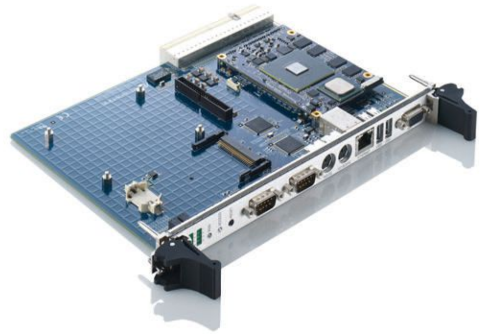
A6pci8029 is a 6U, single slot CompactPCI CPU board, with the Intel Atom processor.

It features Gigabit Ethernet, VGA, USB, COM and PS/2 keyboard & mouse on the front panel; a CompactFlash socket and a 2.5 inch HDD connector provide flexible storage capabilities.

With many choices of CPU speed and memory size, the A6PCI8029 also supports extended operating temperature range.

FEATURES: Intel Atom Processor up to 1.6GHz, Up to 1GB, DDR2-533 SDRAM • 1x VGA • 1x Gigabit Ethernet • 4x USB 2.0 • 2x Serial port RS-232C • PS/2 Keyboard & Mouse • CompactFlash • 1x IDE • Compliant with PICMG 2.0 R3.0 Specifications • 6U size single slot

cpci@eurotech.com **advancedtca-systems.com/p46817**



EUROTECH **A6pci7508 – CompactPCI 6U board with PowerPC**

The A6pci7508 is a 6U high-performance CompactPCI single board computer with an onboard PowerPC® G4 MPC7447A. The A6pci7508 can use either a CompactPCI system slot or a peripheral slot with automatic slot recognition. For very high processing loads, multiple CPU boards can be added to increase the computational performance.

The A6pci7508 is available with a CPU frequency of 600MHz or 1GHz and memory sizes of 512MB or 1GB with ECC support.

cpci@eurotech.com **advancedtca-systems.com/p44193**

EUROTECH **A6pci8026 – 6U CompactPCi with Intel EP80579**

The A6pci8026 is a 6U CompactPCI board sporting a 1.2GHz Intel EP80579 System on Chip. One remarkable feature of the A6pci8026 is the support for up to 2GB of PC2-4200-compatible ECC SO-RDIMM. A rich set of I/O interfaces complements this board making it the ideal foundation for demanding applications where reliability is a must.

FEATURES: DDR2 SDRAM SO-RDIMM, max 2GB, ECC support • 3x GbE • 2x USB 2.0 • 2x SATA 1.0A • 1x PMC slot • 1x VGA • 1x CF • PICMG 2.0 Rev 3.0 compliant

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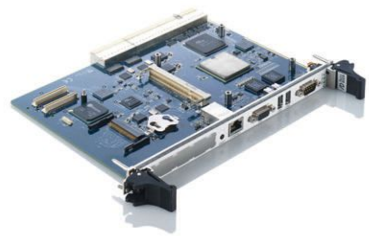


MEN Micro GmbH **D602**

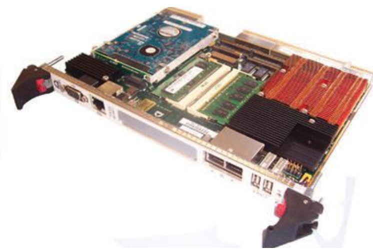
1-slot CompactPCI system slot card • Triple redundancy on a single board • 3x redundant PowerPC 750 CPU, up to 900 MHz • 3x redundant 512 MB DDR RAM • 2x redundant 256 MB Flash, ECC • 1x 1 MB FRAM, ECC • Redundant local PSUs • 1x standard PMC slot • 1x PMC slot for AFDX PMC (rear I/O only) • 1x RS232, PMC I/O, board management and more via rear I/O • Compliant with DO-254 up to DAL A • -40 °C to +55 °C with qualified components

www.menmicro.com **advancedtca-systems.com/p45232**

Pinnacle Data Systems, Inc. **CP86-N1 Intel Core™ 2 Duo Processor Blade**

PDSi's Intel-based CompactPCI x86 Processor Blade (CP86-N1) provides a robust, high-performance general purpose compute platform for use in CompactPCI PICMG 2.16 systems. This latest addition to PDSi's ComputeNode™ family of carrier-grade CompactPCI solutions is built around Intel's 45nm technology "Penryn" Core 2 Duo processor and server-grade "Eagle Lake" chipset (5100 MCH / ICH9R) supporting ECC memory. This powerful, compact blade offers the highest performance and dependability in its class. The ComputeNode CP86-N1 blade includes a standard PMC/XMC site for I/O expansion and features an onboard SATA drive plus high resolution graphics.

info.sales@pinnacle.com **advancedtca-systems.com/p41921**



Kontron **CP6930 and CP3923 switches**

The Kontron CP6930 is a 6U hot-swappable CPCI and VITA 31 switch with 26 GbE ports and 6 high -performance uplinks (10 GbE). Six SFP+ front ports running at 10Gb/s full line speed and 2 SFP ports at the front providing 1Gb support gives flexibility and an intrinsic value for today's investments.

The Kontron CP3923 is a fully managed layer 2/3 Gigabit Ethernet switch offering IPv4/IPv6 routing and full management capabilities. It supports a powerful set of CLI, Telnet, Web and SNMP management interfaces, Layer 2 and Layer 3 (IPv4/IPv6) protocols, Multicasting, QoS and Security.

www.kontron.com **advancedtca-systems.com/p46586**

NEI **N-2710**

NEBS Level 3 certified carrier-grade rack mount server based on Dell PowerEdge technology with integrated GE packet processing technology for network security applications. This DC-powered 2U carrier grade platform contains GE OCTEON-based PCIe IP packet processor cards designed to perform DPI for security gateway applications such as content inspection, data security encryption/decryption (SSL/IPSec/TLS), network monitoring, lawful interception and traffic management. Dual socket support for Intel Xeon 5600 Series 6-core processors and combines high performance with power efficiency to deliver improved performance-per-watt over previous generation rack-mount servers. This rugged server is designed for demanding telco CO environments, network data centers, and enterprise networks. Up to 8 2.5-inch SAS drives with RAID levels 0/1/5/6/10 for maximum reliability and includes hot swap hard drives and redundant 870W DC power supplies for high availability. With ability to install up to four PCIe I/O cards, VARs, ISVs, and TEMs, OEMs can deliver lower-cost communications solutions with value-add services.

www.nei.com **advancedtca-systems.com/p46555**

Kontron **OM9140 14-Slot 10GbE ATCA Platform**

The Kontron OM9140 series of 10GbE ATCA application-ready platforms offers carrier-grade, high-density solutions across a common platform capable of being converted into dedicated or cross-functional network elements for 3G and 4G wireless, IMS, IPTV, and core network applications. Kontron is currently assisting our TEM clients in a multi-phase migration program that prepares them to develop immediately with 40G-ready AdvancedTCA platforms and within a timetable that meets all the technical, cost, and revenue needs of our carrier and service provider clients.

www.kontron.com **advancedtca-systems.com/p46579**

NEI **E-2710**

A purpose-built, highly efficient DC-powered application platform made for power efficient environments. Its core Intel Xeon 5500 series processor better scales power usage to the workload for more energy efficiency. Highly available, open-standard application platform that delivers the speed, computing power and flexibility. Meets demand for green-compliant data center and carrier-class CO technologies. Can host NEI's Element Manager, a s/w tool used to monitor, manage, update and backup/restore the application, OS and associated drivers. This patch management tool streamlines support processes and speeds deployments to simplify platform support throughout its life cycle for a real competitive advantage.

www.nei.com **advancedtca-systems.com/p43806**

Pinnacle Data Systems, Inc. **SKiNET M3000 Mobile Satcom System**

The SKiNET platform offers a compact computing core designed around AMD's x86-based Socket S1 Sempron™ 2100+ processor in a rugged system built around the CPU module that provides both secure and non-secure communication capabilities, with a decent battery run-time and a wide range of AC and DC operating voltages. The SKiNET M3000 system provides exceptional operational flexibility for first responder or mission-critical field communication needs. The platform is also FAA carry-on sized and dual system configurable. Customization and ruggedization welcomed!

info.sales@pinnacle.com **advancedtca-systems.com/p45809**

E-cast SPOTLIGHT

40G and beyond: Next-gen network design with AdvancedTCA

By Warren Webb

Warren Webb, OpenSystems Media (OSM) Technical Editor attended an OSM E-cast in a November 2nd, 2010 E-cast on **40G and Beyond: Next-Gen Network Design with AdvancedTCA.** *Sponsored by the Intel Embedded Alliance, the E-cast featured a panel of experts discussing the latest hardware, software, and standards necessary to support the rapid rise in the number of connected devices.*

Curt Schwaderer, *CompactPCI AdvancedTCA & MicroTCA Systems* Technology Editor, moderated the event for OpenSystems Media. Panelists presenting were: John Long, Product Line Manager for ATCA Products at RadiSys Corporation, Brian Carr, Strategic Marketing Manager at Emerson Network Power, Paul Stevens, Telecom Sector Marketing Director at Advantech, and Sven Freudenfeld, Business Development for Telecom at Kontron.

Curt opened the E-cast with insight into the enormous growth of mobile Internet bandwidth usage. He cited projections from Cisco that forecast a compound annual bandwidth growth of over 100 percent in almost every region worldwide from 2009 to 2014. Curt also referenced an iSuppli Corporation report stating that capital expenditures for wireless infrastructure will once again be on the rise in 2011 after having been delayed due to the global recession.

John Long of RadiSys then described how Long Term Evolution (LTE) applications are driving requirements for 40G. Although LTE represents simplified network architecture there are a lot of complications and potential security risks that must be addressed. John addressed the question of using Intel architecture in current LTE control plane applications and referenced a timeline for using Intel architecture to address higher complexity packet processing applications.

Brian Carr of Emerson Network Power presented an introduction to the AdvancedTCA open standard and how it covers shelves, board, mezzanines, power distribution, and system management. Brian also described the technical differences between 10G and 40G architectures and the associated challenges. An evolution path to 40G was detailed for customers that already employ 10G AdvancedTCA. This path includes the deployment of 40G backplanes, switch hubs, and payload blades as necessary to support new services or higher capacity options for existing systems.

Paul Stevens of Advantech covered system scalability in enterprise and carrier networking. He outlined the network and software elements to consider when scaling from 10G to 40G and beyond to possibly 100G throughputs. He dissected the anatomy of a current network appliance and covered the techniques and resources necessary to translate to a scalable blade topology and then to extend that with full 40G interconnects.

The last speaker, Sven Freudenfeld of Kontron, offered additional approaches to take full advantage of multicore and AdvancedTCA. Starting with multi-core, Sven covered the hardware and software extensions that are bringing new opportunities and capabilities to AdvanecdTCA. Virtualization allows users to consolidate multiple applications into one platform and share resources such as processor capabilities and storage between individual blades. Users can also apply virtualization on top of AdvancedTCA to combine multiple applications into a single blade.

Excerpts from the panel discussion

The question and answer portion of the E-cast began with a panel discussion of questions submitted by the attendees. Following are excerpts from that session.

CS: ***What do you see as some of the biggest challenges for the success of 40G ATCA moving forward?***

SF: There are a couple of items in terms of launching products including having all the components available. Designers must start with the backplane approach itself, implementing the IEEE specification. PICMG is currently finalizing their specification and that platform is becoming widely available. The latest ATCA framework is really just considered infrastructure to support bandwidth to each of the individual blades. When it comes down to the blades, the software component is the key element to make it happen and to take full advantage of the infrastructure of the ATCA platform. The challenge is to basically combine all of this together and achieve the fastest time to market with the platform itself.

CS: ***When do you see volume 40G adoption kicking in and how fast or slow is 100G behind it?***

JL: When you look at 40G adoption you have look at how Brian set it up. Chassis that support 40G are being deployed today. You will see switches starting to be deployed next year and payload blades also next year. I don't think we will see mass deployment in the carrier network until sometime in 2012 or 2013. Before you see mass adoption you will see a year or two in the development labs. And we think the start of that curve will be next year. Much like the adoption of 1G to 10G – it takes time.

CS: ***Are there any wireless and wire line service providers doing any kind of in-lab tests and trials at this point or are the pieces just not there yet?***

JL: We are just starting to get there so it is too early for the carriers to get a full 40G platform with the components that are available. And with 100G we are starting to see people really pushing the technology. We still have challenges on the silicon side. Our expectation is that five years from now we will start seeing some migration to 100G.

CS: ***What is the industry doing to address the interoperability concerns at 40G for software, blades, backplanes, and shelves?***

PS: I really believe this is where PICMG and the Communications Platforms Trade Association (CP-TA) are working with their members to create the best environment to make interoperability work. The CP-TA interoperability and compliance documents were put together to define test methodologies for various platforms. They are really the result of multivendor cooperation to insure that the products work together without major challenges to any of them. We all work together at plugfests as well. Another one was held just a couple of weeks ago in Germany. That also helps to insure that the widest range of products work together and mitigate problems.

CS: ***Since 40G payload blades won't be available until next year, why should service providers worry about 40G ATCA right now?***

BC: It all has to do with smooth migration. The earlier you prepare, the smoother it will be. So if you are hoping to take advantage of 40G ATCA, and you are currently deploying 10G ATCA, then now is the time to think about getting ready. Remember, as I said, the first thing that you need to do is to introduce 40G ready platforms with suitable backplanes and I think most people understand that. And after that you can gracefully introduce 40G switches and payload as you are ready. Remember you can get those platforms now. The 40G switches will port existing 10G payloads and a mix of 40G and 10G payloads. So yes, you should think about it now.

CS: ***Is there is a plan to support 100G over the backplane?***

BC: We've already seen situations where people are talking about it. We're looking to the future. I've already mentioned that people that are pushing the edges are already deciding what the next step is. But what we need to be careful of is: There is no IEEE standard for 100G on the backplane yet. The switches themselves would need another major increase in capacity to do that and we are a fair way away from payload technology that could effectively process 100Gs worth of traffic for any slot. So I don't see 100G ATCA superseding 40G ATCA any time soon. I do believe we will see 100G coming in, but it will be as options for network terminations on the switch hub. That's likely to be the first.

JL: I think Brian summed it up very well. Network interfaces will be first, but over time you will see customers demand 40G over the backplane. There are technical issues and standards issues to address, but in time it will come.

PS: I agree with what my colleagues just said. What we are beginning to see now is people are looking at bringing in 100G through the switch. We're probably still a long way off from seeing 100G within the system itself.

CS: ***What percentage of the new Telecom Equipment Manufacturers (TEMs) will remain proprietary versus ATCA? I know the ATCA evolution has been happening within telecom for quite a while. How do you see the conversion to ATCA within TEMs within the next few years?***

JL: If you look at TEMs overall, a vast majority of them have ATCA somewhere in their portfolio. You also have to look at where ATCA makes sense. For applications like the eNodeB, ATCA is probably not the right solution. Where we think it makes sense, where the bandwidth and cost points make sense, we expect ATCA to continue to grow.

BC: Yes, I go along with that. I think the other point to bring out is that ATCA is an open standard and there are quite a lot of TEMs who have adopted ATCA and they still make it all themselves. So a lot of companies that are on this call don't necessarily sell to those people. But the whole point is that ATCA is an open standard so you can start and you can take advantage of the ecosystem, and the ecosystem is an incredibly powerful thing.

SF: Yes, I think that the adoption rate and the fact that ATCA is an open standard is very well recognized and multiple TEMs have been launching products. There has been a lot of consolidation within the TEMs market itself by mergers and acquisitions. But the advantage is that most of them have already used ATCA in the past and now moving to 40G gives a much broader application arena for ATCA. It helps them not only to consolidate platforms, but also to get new platforms to the market on time to make revenue.

CS: ***How about blade computer platforms using ATCA with 40G. We saw a lot of architecture diagrams from you folks about 1 or 10G into the blade. Are any of them going to use 40G or is that just a switch pipe?***

JL: I'm not sure if you'll see 40G on a compute blade in the next generation. I think that if you look at the packet processing blades, you will see 40G.

PS: Yes, we are seeing 40G at the switch end of things now. It is becoming mainstream in PCI now. 40G into the switch with multiple connections.

BC: We can see both situations in place. Fundamentally, there's still going to be a fair cost differential between 10G and 40G, which means that there is going to be a place for both 10G and 40G blades in the portfolio. So the ones that are focused clearly and heavily on server side applications will generally stay on 10G whereas the ones that are focused more clearly on packet processing applications will move to 40G more quickly.

SF: There is a combination of that leveraging 40G. If you look at MME platforms for example the security and data gateway functions are the key. The best combination already is in the space of being deployed for the 10G. The 40G gives much broader bandwidth and takes full advantage of the all IP infrastructure. There are a couple of items to consider. One of them is the over speed synchronization infrastructure. But, I agree on the cost point. Some of the data frame functions are really not needed but they end up in deep packet inspection functionality where the combination of multi-core and the software can help to keep the cost reasonable and also reuse some of the hardware architecture that is already deployed.

CS: ***Where is the point at which Intel architecture can capably handle the packet processing data plane functions? It that today or is it next year?***

JL: If you look out there, in some applications, Intel can handle the packet processing and it depends on the functionality and data planes. And over time the amount of applications and the density that the x86 architecture can address will increase.

BC: I think John has put it very well there. In fact, we are already in a situation today where Intel architecture is doing packet processing. So it depends on the rate and the size of the packets as to how far that goes. We can certainly see the next generation coming through and that's going to be very interesting indeed.

PS: I think the combination of the latest software from companies like 6WIND and Wind River are going to help accelerate that. They've already given pretty much a 10x improvement in performance over current applications. On the other side, x86 issues are getting faster, technology refreshes are getting more cores and accelerating the technology. x86 processors are pretty good today for flow analysis, database integration, management and general applications. Fast MPUs are better for packet processing applications, and things like operations and payload identification. I think the pendulum is swinging and there's more refreshes coming with x86. And there's a lot of exciting technology coming out in the next year or so.

Some of the data frame functions are really not needed but they end up in deep packet inspection functionality where the combination of multi-core and the software can help to keep the cost reasonable...

Sven Freudenfeld

SF: I think it has already been well said. I think it matters what you are going to do with a packet and the packet length in terms of performance and dedicated resources on the blade itself. Yes, I completely agree that some of the functions can be done with x86 and also the nice thing on x86s is that some of the operating systems work with packet processing functions. Most likely it needs additional software development. It depends on what types of applications are being created. So we have a niche market where vendors can take advantage of the x86 platform doing some of the data processing functions already.

***Warren Webb** is an internationally known industry analyst and editor. He is the former technical editor of* EDN *magazine. He worked on the magazine's Embedded Webblog commenting on board-level embedded hardware, development tools, and software. Additionally, Warren wrote in-depth technical articles on hardware design, software development, and emerging technologies.*

Register to view the archived E-cast, 40G and beyond: Next-gen network design with AdvancedTCA *with slides and audio at* http://bit.ly/blFol7.